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ORIGINAL ARTICLE

CHARACTERIZATION & SIMULATION OF CLASS AB CURRENT CONVEYOR SECOND GENERATION (CCII) BASED ON CURRENT MIRRORS

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ABSTRACT

Research in analog integrated circuits has recently gone in the direction of low voltage (LV) low-power (LP) design especially in the environment of portable systems. In this area traditional voltage-mode techniques are going to be substituted by the current-mode approach which has the advantage to overcome the gain-bandwidth product limitation typical of operational amplifier. Then they do not require high voltage gains and have good performance in terms of speed bandwidth and accuracy. Inside the current-mode architectures the current-conveyor (CCII) can be considered the basic circuit block because all the active devices can be made of a suitable connection of one or two CCIIs. Recent advances in integrated circuit technology have also highlighted the usefulness of CCII solutions in a large number of signal processing applications. This project describes different topologies of CCIIs. All topologies have been simulated in different CMOS process technologies using Eldo Spice tool and layout is made using Mentor Graphics Back End tools like IC Station and DA-IC. Different characteristics such as gain, bandwidth, terminal impedances, slew rate, dynamic range, input-output current characteristic and offset are measured and tabulated for all the CCII topologies.

Keywords: gain,bandwidth,terminal impedances, slew rare, dynamic range, current mode techniques, voltage mode techniques.

1.INTRODUCTION

In analog circuit design, there is often a large request for amplifiers with specific current performance for signal processing. The current-mode approach [1],[2] considers the information owing on time-varying currents. Current-mode techniques are characterized by signals as typically processed in the current domain. Current-mode circuits have some recognized advantages. Firstly, they do not require a high voltage gain, so high performance amplifiers are not needed. Then, they do not need high precision passive components, so they can be designed almost entirely with transistors. This makes the current mode circuits compatible with typical digital processes. Finally, they show high performance in terms of speed, bandwidth and accuracy. The current-mode approach is also powerful if we consider that all the analog IC functions, which traditionally were been designed in the voltage-mode, can be also implemented in current-mode. In analog circuit design, there is often a large request for amplifiers with specific current performance for signal processing. The current-mode approach [1],[2] considers the information owing on time-varying currents. Current-mode techniques are characterized by signals as typically processed in the current domain. Current-mode circuits have some recognized advantages: firstly, they do not require a high voltage gain, so high performance amplifiers are not needed. Then, they do not need high precision passive components, so they can be designed almost entirely with transistors. This makes the current mode circuits compatible with typical digital processes. Finally, they show high performance in terms of speed, bandwidth and accuracy. The current-mode approach is also powerful if we consider that all the analog IC functions, which traditionally were been designed in the voltage-mode, can be also implemented in current-mode.

2. CURRENT CONVEYOR(CC) SECOND GENERATION

The current conveyor (CC) is a basic block that can be implemented in analog circuit design using a like-OA approach; it also represents an effective alternative to the same OA for designers. This is mainly due to the fact that both practical current conveyors and OAs are marked by characteristics that are very

close to the ideal ones. Sedra and Smith introduced the current conveyors in 1968 [3],[4] but their real advantages and innovative impact were not immediately clear at that time. Only in recent years, with the growing diffusion of the current-mode approach as a way to design LV LP circuits, current conveyors have gained an increased popularity.

There is only a little difference between the two blocks, but in the practical applications CCII has shown to be much more versatile and helpful than CCI. Figure 1.1 shows the block diagram of CCII.

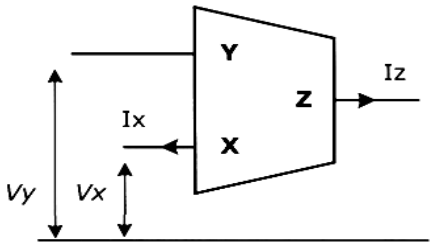

Fig 1.1 Block representation of Current Conveyor II

CCII is topologically very similar to its predecessor .[3],[4]. The electrical characteristics of the new block are reported in Figure 1.2

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

CCII Node	Impedance Level
X	Low (ideally 0)
Y	High (ideally ∞)
Z	High (ideally ∞)

Fig 2.2 Current Conveyor II Main Characteristic

Compared to the previous version, the innovation of CCII is represented by the absence of current in the Y node, owing to its high impedance (ideally infinite). Using this model, currents owing at X and Z nodes are equal in magnitude but opposite in direction, assuming CCII as their reference. This means that if Ix flows out from X node, Iz flows into Z node and vice versa. On the other hand, real CCII implementations can lead to two different situations, as for CCI. If Ix and Iz flow in opposite directions from the CCII point of view, the block is called negative CCII (CCII-) while, when Ix and Iz flow in the same direction, we have positive CCII (CCII+). After this statement, it is clear that Figure 1.1 represents a CCII+. More complete nullator-norator model for CCII, which takes into account the two possibilities described above, is represented in Figure 2.3 [3].

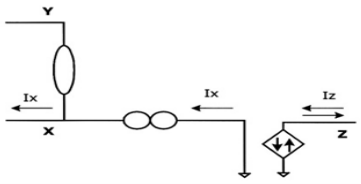

Fig 2.3 Nullator-norator CCII Model

3. CCII TOPOLOGY

The nMOS transistor can be regarded as a CCII as shown in Figure 3.1. This not only gives the idea of the importance and usefulness of CCII but also introduces a particular analogy between transistor and conveyor [3].

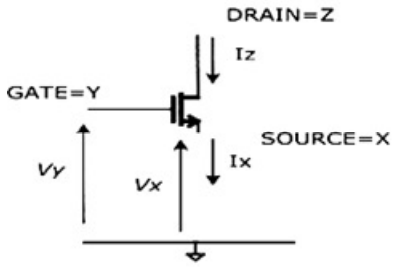

Figure 3.1 nMOS transistor and its equivalence with CCII

Owing to the source follower effect the signal applied to Y node (MOS gate) is almost equal to that obtained at X node (source) as expressed by the following parameter which represents the node X-Y voltage transfer function:

Ix and Iz currents are equal as cleared from the small signal equivalent circuit of the nMOS transistor shown in Figure 3.2 . The ratio between these currents is expressed by the following parameter which is exactly equal to 1 in this analogy:

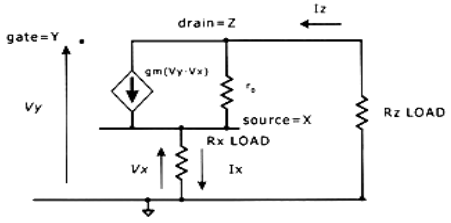

Figure 3.2: Small Signal Circuit for nMOS

Impedance level at Y node is given by the transistor gate capacitance so it is quite high as required by theoretical specifications. X node impedance value is affected by the load connected to Z node while the impedance seen at Z terminal is related to the load connected to X node. In particular being a constant parameter whose value is 2/3 in saturation region and 1 otherwise W and L width and length of the MOS respectively and the unitary gate capacitance we have:

A single MOS transistor can be seen as a second generation current conveyor considering small input signals but biasing voltages at X and Y show a relative difference of about one threshold voltage. This

difference can be eliminated considering a traditional nMOS current mirror which can also be seen as a CCII as shown in Figure 3.3 [3].

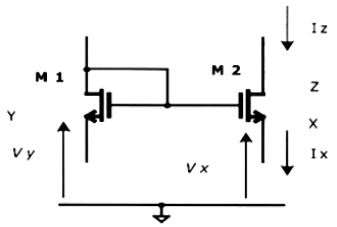

Figure 3.3: CCII characteristics in nMOS current mirror

For this circuit the current transfer function and the impedance levels at X and Z node are the same as presented in equations (3.2) (3.4) (3.5). The Y node impedance is given from Figure 3.4 as under:

$$Z_Y = R_{IBIAS2} \parallel \left(\frac{1}{g_{m1}} + R_{IBIAS1}\right) \qquad (3.6)$$

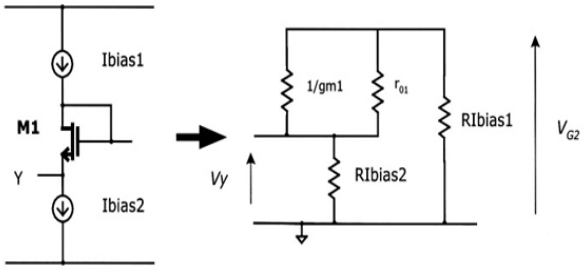

Figure 3.4: Half nMOS current mirror and its small signal equivalence

The voltage at X node can be expressed as a function of the voltage at M2 gate (V_{G2}) as follows:

$$\frac{V_X}{V_{G2}} = \frac{g_{m2} r_{02} R_{XLOAD}}{1 + g_{m2} r_{02} R_{XLOAD}} \cong 1 \qquad (3.7)$$

To determine parameter, V_{G2} can be expressed in terms of as a function of V_Y considering the circuit shown in Figure 3.4.

$$V_{G2} = \frac{R_{IBIAS1}}{R_{IBIAS1} + \frac{r_{01}}{1 + g_{m1} r_{01}}} V_Y \cong V_Y \qquad (3.8)$$

From eq.3.8 it comes that the voltage V_{G2} is equal to the one applied at Y node only if the biasing sources show a large output resistance. In this way, we obtain the same formula for parameter (equation 3.1).In Figure 3.2, a negative CCII has been implemented. If a positive current conveyor is needed, it is possible to add a current mirror as pictured in following figure. In this topology, Ix and Iz flow in the same direction with respect to the CCII, so performing the CCII+ operation.

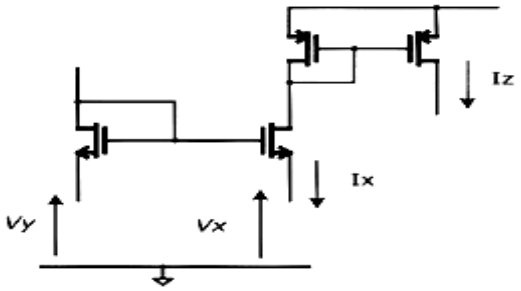

Figure 3.5: Current Mirrors used for Positive CCII

The topology presented in Figure3.5 can be "doubled" to obtain a class AB current conveyor depicted in Figure 2.22. In this circuit, obviously, IBias1 and IBias2 have to be equal [5],[6].

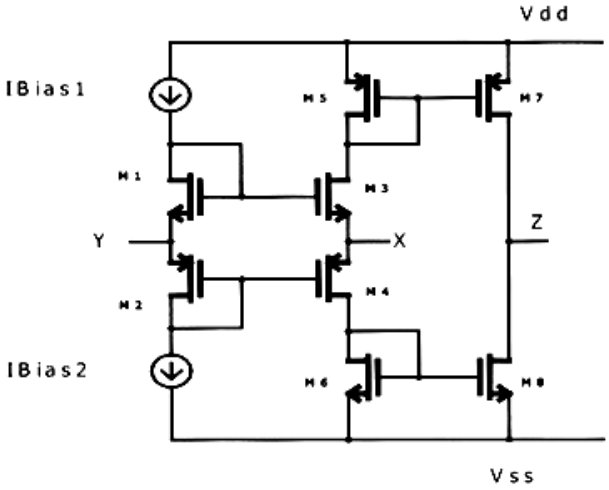

Figure 3.6: Class AB CCII based on Current Mirrors

4. CLASS AB CCII BASED ON CURRENT MIRRORS

4.1 Class AB CCII based on Current Mirrors

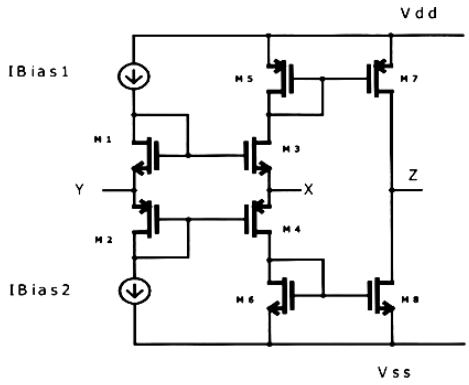

Figure 4.1: CCII Based on Current Mirrors

Now the above topology is implement using different CMOS technologies like 0.05µm,0.18µm,0.25µm and 0.35µm.After getting the simulation result for different parameters like off-set voltage, input-output impedande,bandwidth and power consumptions, a conclusion is derived by comparing the above parameters with different CMOS technologies.

3.2 Pre-Layout Simulation Results

For the CCII depicted in Figure 4.1, pre-layout simulation results using ELDO SPICE tool of Mentor Graphics are shown below:

*Simulation Results for AMI 0.05µm CMOS Technology

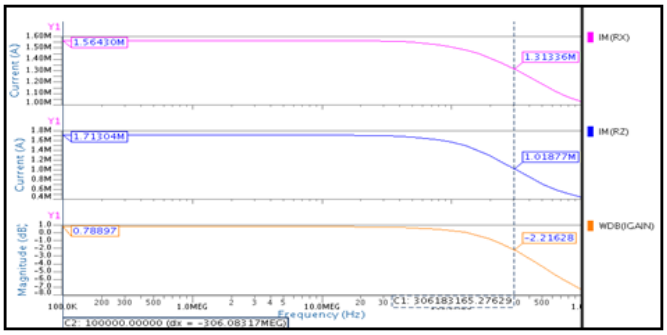

Figure 4.2: Gain and Bandwidth for 0.05µm CMOS technology

The bandwidth is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

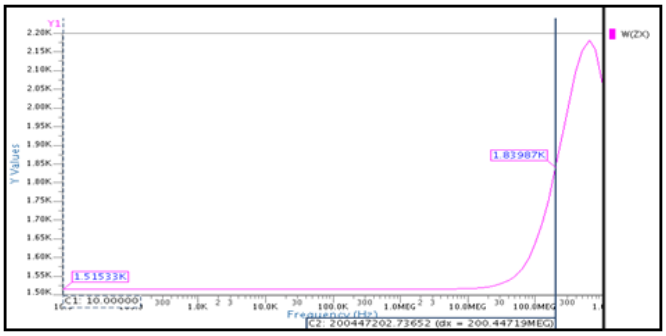

Figure 4.3: Impedance at X node for 0.05µm CMOS technology

The X terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz)at X terminal with terminating resistors of 1K at Y and Z terminals.

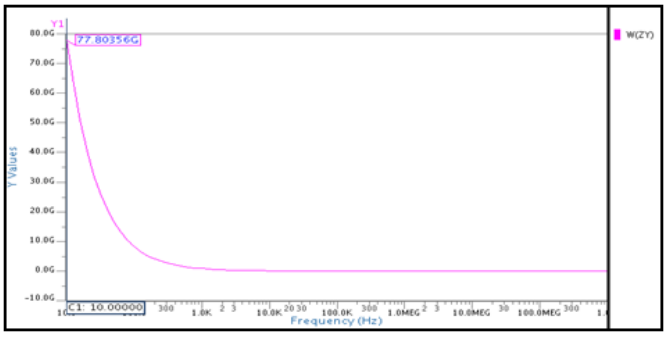

Figure 4.4: Impedance at Y node for 0.05µm CMOS technology

The Y terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

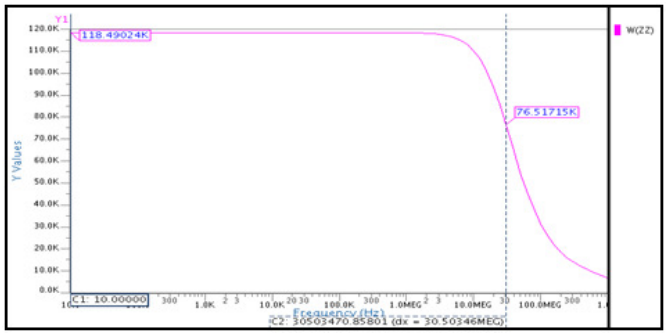

Figure 4.5: Impedance at Z node for 0.05µm CMOS technology

The Z terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Z terminal with terminating resistors of 1K at X and Y terminals.

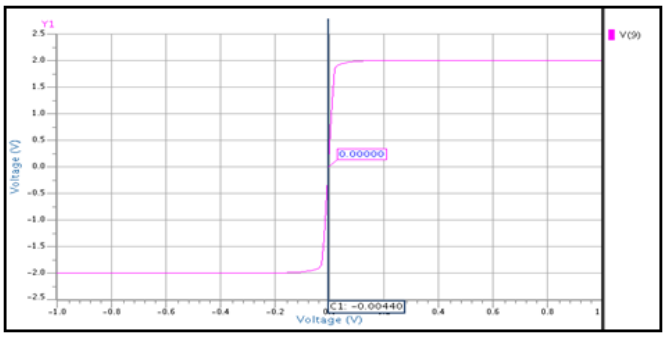

Figure 4.6: Offset for 0.05µm CMOS technology

The offset is measured by varying the dc voltage applied at Y terminal and plotting the Z terminal voltage variations. During this observation, the X terminal is grounded.

*Simulation Results for TSMC 0.35µm CMOS Technology

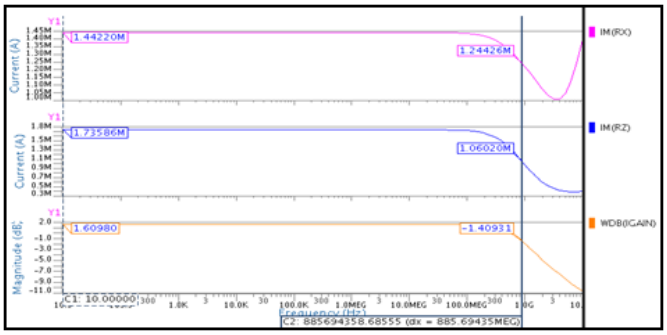

Figure 4.7: Gain and Bandwidth for 0.35µm CMOS technology

The bandwidth is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

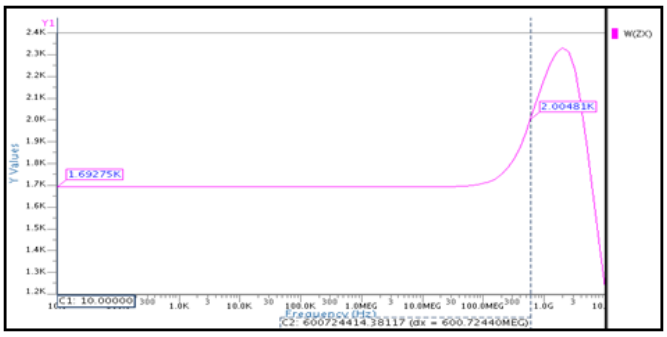

Figure 4.8: Impedance at X terminal for 0.35µm CMOS technology

The X terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at X terminal with terminating resistors of 1K at Y and Z terminals.

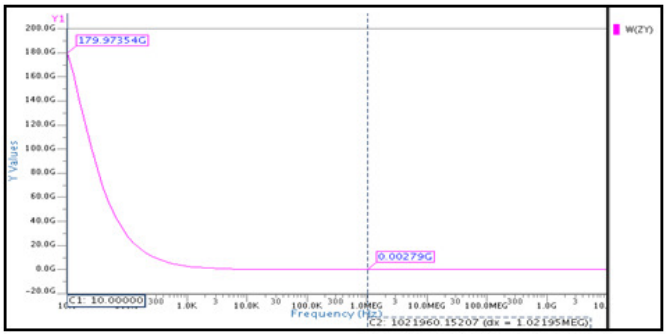

Figure 4.9: Impedance at Y terminal for 0.35µm CMOS technology

The Y terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

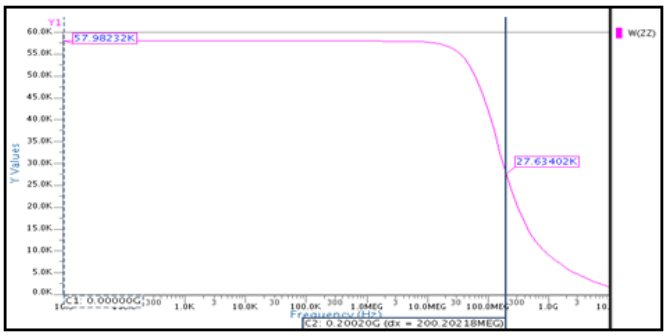

Figure 4.10: Impedance at Z terminal for 0.35µm CMOS technology

The Z terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Z terminal with terminating resistors of 1K at X and Y terminals.

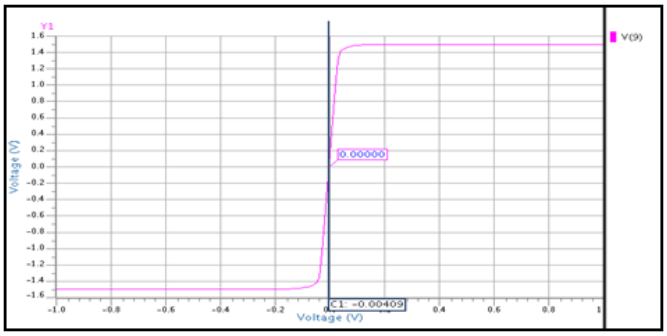

Figure 4.11: Offset for 0.35µm CMOS technology

The offset is measured by varying the dc voltage applied at Y terminal and plotting the Z terminal voltage variations. During this observation, the X terminal is grounded.

*Simulation Results for TSMC 0.25µm CMOS Technology

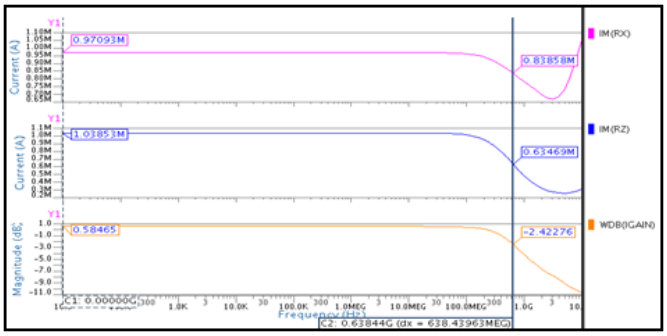

Figure 4.12: Gain and Bandwidth for 0.25µm CMOS technology

The bandwidth is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

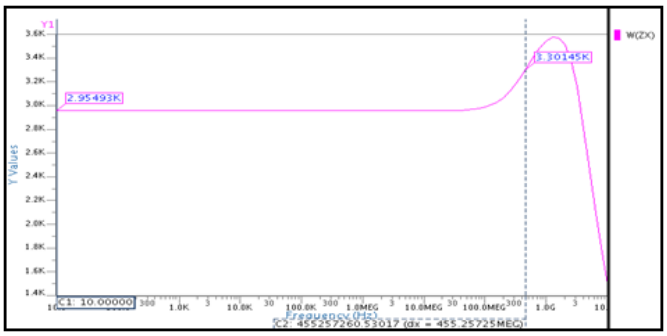

Figure 4.13: Impedance at X terminal for 0.25µm CMOS technology

The X terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at X terminal with terminating resistors of 1K at Y and Z terminals.

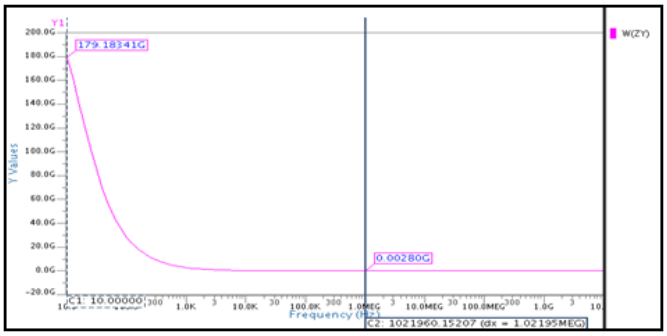

Figure 4.14: Impedance at Y terminal for 0.25µm CMOS technology

The Y terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

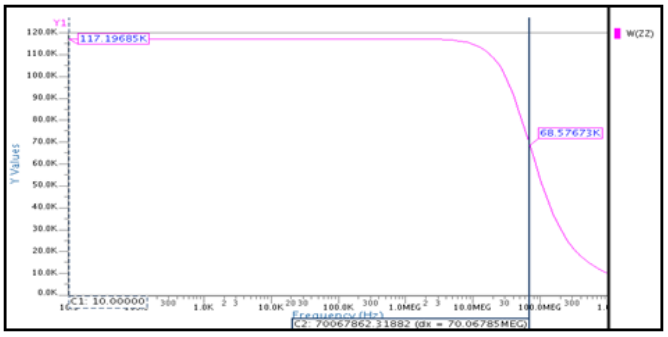

Figure 4.15: Impedance at Z terminal for 0.25µm CMOS technology

The Z terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Z terminal with terminating resistors of 1K at X and Y terminals.

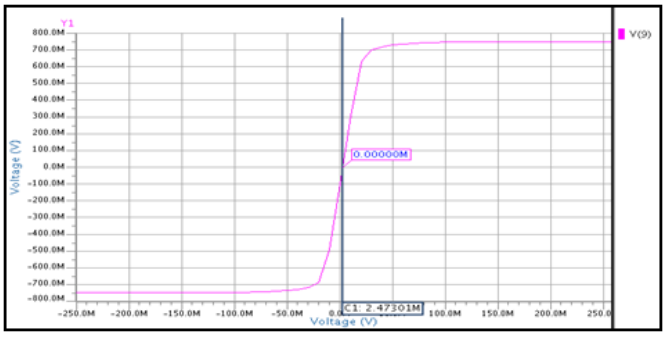

Figure 4.16: Offset for 0.25µm CMOS technology

The offset is measured by varying the dc voltage applied at Y terminal and plotting the Z terminal voltage variations. During this observation, the X terminal is grounded.

*Simulation Results for TSMC 0.18µm CMOS Technology

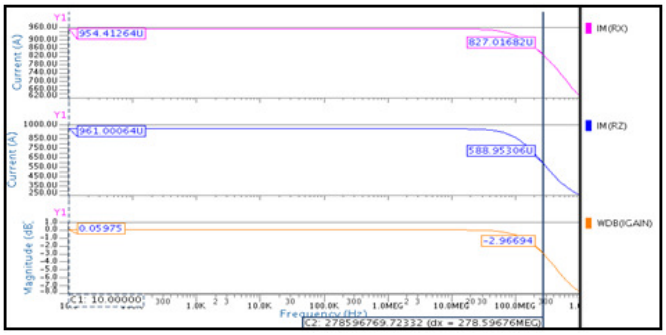

Figure 4.17: Gain and Bandwidth for 0.18µm CMOS technology

The bandwidth is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

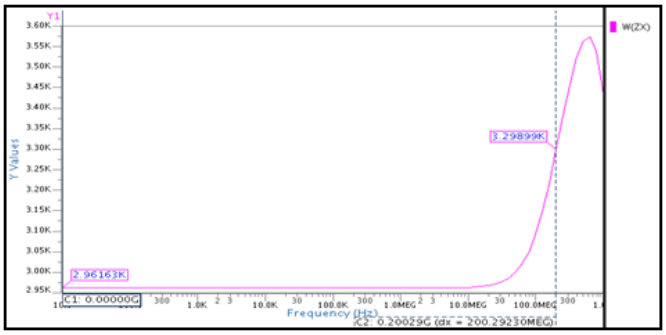

Figure 4.18: Impedance at X terminal for 0.18µm CMOS technology

The X terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at X terminal with terminating resistors of 1K at Y and Z terminals.

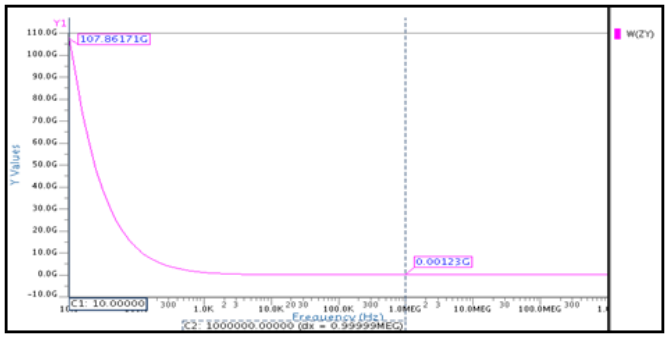

Figure 4.19: Impedance at Y terminal for 0.18µm CMOS technology

The Y terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Y terminal with terminating resistors of 1K at X and Z terminals.

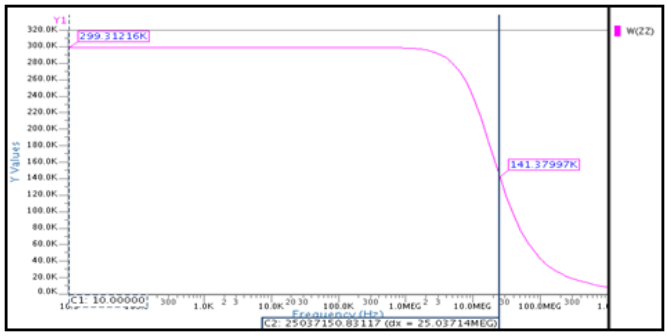

Figure 4.20: Impedance at Z terminal for 0.18µm CMOS technology

The Z terminal impedance is measured by applying a sinusoidal signal (0.5mV,1MHz) at Z terminal with terminating resistors of 1K at X and Y terminals.

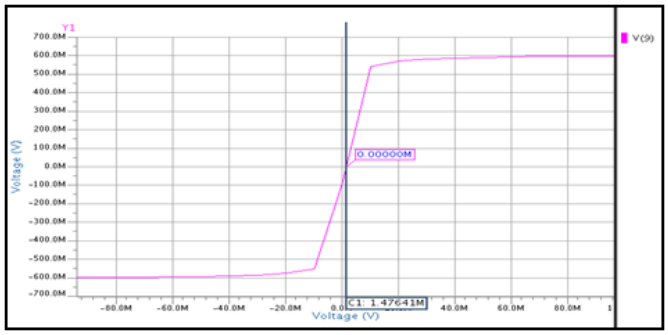

Figure 3.21: Offset for 0.18µm CMOS technology

The offset is measured by varying the dc voltage applied at Y terminal and plotting the Z terminal voltage variations. During this observation, the X terminal is grounded.

5.CONCLUSION

Class AB CCII based on current mirror is implemented and simulated using different CMOS technologies. From the above simulation it is derived that different CMOS technology give different result for different parameters. As we will seen in table derive below, we can optimized some of the parameters using different CMOS technologies.

Table 5.1: Transistor aspect ratios for class AB CCII based on Current Mirrors

Transistor aspect ratios				
Transistors	W(µm) / L(µm)			
	0.05µm	0.35µm	0.25µm	0.18µm
M1,M3,M6, M8	20/1	7/0.35	5/0.25	7.2/0.36
M2, M4, M5, M7	60/1	21/0.35	15/0.25	21.6/0.36

Table 5.2: Characteristics of Class AB CCII based on Current Mirrors

Current Conveyor Characteristics				
Data & Parameters	Simulated Value			
	0.05μm	0.35μm	0.25μm	0.18μm
Supply Voltage	±2.0V	±1.5V	±0.75V	±0.6V

Power Dissipation	283μW	167μW	37.93μW	26.78μW
3dB Bandwidth	306MHz	885MHz	638MHz	278MHz
Biasing Current IBIAS	26μA	20μA	10μA	8μA
Offset	-4.40mV	-4.09mV	2.47mV	1.47mV
Current Gain(ß)	1.095	1.204	1.069	1.007
Node Y Parasitic Impedance	78$G\Omega$	180$G\Omega$	179$G\Omega$	108$G\Omega$
Node X Parasitic Resistance	1.52$K\Omega$	1.69$K\Omega$	2.95$K\Omega$	2.96$K\Omega$
Node X Parasitic Inductance	1.46μH	0.53μH	1.15μH	2.62μH
Node Z Parasitic Resistance	118$K\Omega$	58$K\Omega$	117$K\Omega$	299$K\Omega$
Node Z Parasitic Capacitance	0.068pF	0.029pF	0.033pF	0.045pF

from the above table we can conclude that different parameter can optimized using different CMOS technologies. Power is the essential requirement for any device and chip. We get the minimum power dissipation using 0.18μm CMOS technology which is the essential requirement for any chip and devise. Offset voltage is also minimized using 0.18μm CMOS technology with camper to other technology which is the essential requirement for getting output with minimum redundancy. bandwidth is maximum in 0.35μm technology.

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