Golden Research Thoughts
ISSN 2231-5063
Impact Factor : 2.2052 (UIF)
Volume-4 | Issue-2 | Aug-2014 Available online at www.aygrt.isrj.net

A HIGH RELIABILITY SINGLE-PHASE BOOST RECTIFIER SYSTEM FOR DIFFERENT LOAD VARIATIONS

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Abstract :- Pulse width modulation rectifiers are extensively used in battery charger, regulated dc voltage source, UPS systems, static frequency changer and ac line conditioner, where the main requirements are unidirectional power flow, regulated output dc voltage and near unity input power factor. In case of single switch boost rectifier, additional requirement of dc bus voltage balancing is essential. The conventional control techniques involve complex mathematical operations, which increase the cost and complexity of the controller. Simple control schemes based on constant-switching-frequency resistance emulation control, which do not require any of the above operations, are developed here for PWM boost rectifier. All the necessary control operations are performed without using multiplication, division and square-root operation. The power circuit of the proposed converter can be configured either for DCM or for CCM by simple on–off control of an auxiliary switch. Similarly, the proposed control circuit can also be configured either for CCM or for DCM simply by choosing the appropriate carriers.

Keywords:- Continuous-conduction-mode (CCM), dis-continuous-conduction-mode (DCM).

I. INTRODUCTION

Power electronic converters can be broadly classified as AC-DC, AC-AC, DC-AC and DC-DC converters. The focus of the work presented in this thesis is in the AC-DC conversion. Most AC-DC converter applications desire a constant DC output voltage which will be further used for other purposes. Till very recently the attention of all manufacturers and users of AC-DC converters was on the DC side with the most popular AC-DC converter being rectifier with C filter at lower power levels and the phase-controlled rectifier with LC filter at higher power levels.

Currently, the concern in rectifiers includes power quality issues relating to the source end as well. The reason for this is the undesirable AC line current harmonics drawn from the utility by the

standard rectifiers. The presence of harmonics in the line current results in the distortion of the voltage at the Point of Common Coupling (PCC) due to the presence of source inductance. This may cause malfunction of other loads, power system protection and monitoring devices. Some of the other problems caused by line current harmonics are, overheating of the neutral line, interference with communication and control signals etc. With presence of lower-order harmonics in input current, power factor comes down. Poor power factor of operation implies ineffective use of the volt-ampere rating of the utility equipment. These problems have resulted in the additional concern relating to source current quality.

With the advent of fast semiconductor devices such as MOSFET and IGBT, and the development of various pulse width modulation (PWM) techniques, passive rectifiers are increasingly replaced with PWM rectifiers. The important advantages of the PWM rectifiers over the passive rectifiers are given below:

(i) Sinusoidal input current operation. (ii) Adjustable input power factor. (iii) Regulated output dc voltage. (iv) Low value energy storage elements (inductors and capacitors). (v) Good dynamic response against sudden changes in input voltage and load current. (vi) Higher efficiency of power conversion.

The CCM is preferred over DCM because of continuous input current and low conducted electromagnetic interference (EMI) [6]. However, it is reported to have high input current distortion at light load [7]. For a particular switching frequency and boost inductance, the amount of current distortion increases as the load decreases [7]. A high valued boost inductor is necessary at light load to limit the input current distortion [7]. This increases the size, weight, and cost of the converter and results in poor system dynamic response. Hence, CCM is preferred at higher loads [7], [8].

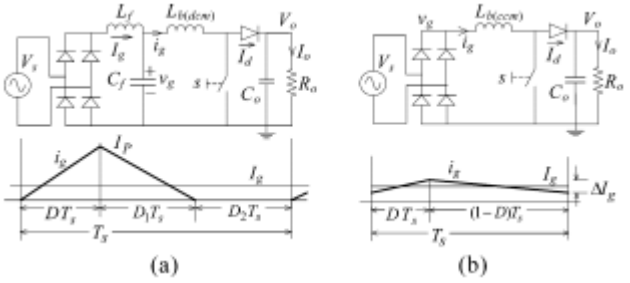

Fig1. Single-phase, single-switch boost rectifier: (a) topology based on DCM and (b) topology based on CCM.

The above issues are not seen, when the converter is operated in DCM. However, DCM is always associated with high device current stress and conducted EMI [6]. Therefore, a high current rated device

and a costly EMI filter are necessary at higher loads. Thus, DCM is preferred for light loads.

The present work deals with a constant output voltage application, where the load current varies over a wide range (10% to 110% of rated load current) and the converter is required to comply with the necessary harmonic standards [1], [2]. It can be seen from the above discussion that neither of the operating modes (CCM and DCM) alone is suitable and economical for the above application. Therefore, the optimum choice is to operate the converter in DCM during light loads and in CCM for higher loads [9]. The load boundary between DCM and CCM operations can be set at a suitable level (say 50%) to limit the peak device current stress under DCM up to the rated device current under CCM without using a higher current rated device.

Similarly, the minimum load under CCM, for which the converter is required to comply [1], [2] is 50% rated load. These per-mitts we to use a low valued boost inductor compared to the en-tire CCM case without any degradation in the performance of the converter [9].

The main challenge associated with such a mixed-mode operation [9] is to realize the two distinct operating modes (DCM and CCM) into a single converter system without introducing any appreciable dynamics during transition between the two operating modes. There are two possible ways to achieve this. The first method suggests a single-valued boost inductor with constant but two different switching frequencies (a low switching frequency for DCM and a high switching frequency for CCM) for the above operation. The second method requires two different boost inductors (a high valued inductor for CCM and a low valued inductor for DCM) with a constant switching frequency for above application. The first method is simpler than the second method, as it only requires the switching frequency of the converter to be changed. However, the second method re-quires the physical inductors to be changed.

A converter system, using two different switching frequencies (2.56 kHz for DCM and 25.6 kHz for CCM) and a single valued boost inductor has been reported in [9]. The use of two different switching frequencies introduces difficulties in de-signing the EMI filter. The controller works in the principle of voltage mode control without using any input current sensor. A current sensor is however required for over-current protection of the converter. The input current distortion under DCM is high as there is no low pass filter connected at the input to the converter. The implementation of the above control scheme involves complex mathematic operations, such as multiplications, divisions and square root operations.

A simple, input voltage sensor less, current-mode controller [10] is proposed for the above rectifier system. The controller works in the principle of one-cycle control [7] or the nonlinear carrier control [4], [11] without using any of the above-mentioned complex mathematical operations. The required gating pulses for the converter switch are generated by comparing the measured input current with one of the two periodic carriers in a modulator. A linear carrier is used under CCM, while a non-linear carrier is selected under DCM. The measured load current is used to select the desired operating mode (CCM or DCM). A simple load current feedforward scheme is used to improve the dynamic response of the converter system, which also ensures a smooth transition from one operating mode to the

other. The proposed concept has been simulated on MATLAB/SIMULINK platform and experimentally validated on a 600-W prototype. The simulation and experimental results are presented.

II. PROPOSEDSINGLE-PHASERECTIFIERSYSTEM FOR WIDE RANGE OF LOAD VARIATIONS

As previously mentioned, the single-switch DCM and CCM boost rectifier circuits are suitable for lighter and higher loads, respectively. Combining these rectifier circuits, a single-switch boost rectifier, shown in below Fig2, is proposed. This boost rectifier will be termed as single-switch, CCM-DCM boost rectifier

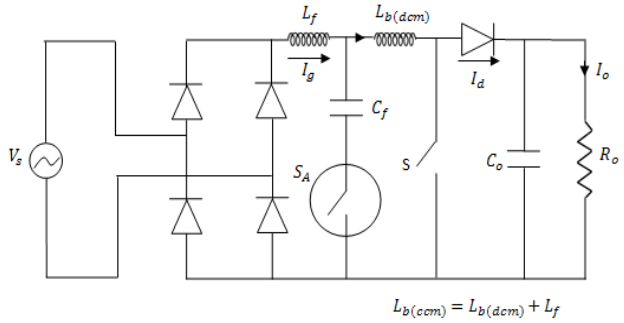

Fig2: Proposed single-switch, CCM-DCM boost rectifier

The switch may be realized by using two anti-parallel thyristors as shown in Fig.2. This configuration ensures smooth transitions between the DCM and CCM operating modes. For example, let us assume that the rectifier is initially operating under DCM, and is now required to be driven into CCM. Under DCM, the instantaneous currents through $L_{b(dcm)}$ and are different (i.e. $i_g \neq$) [see Fig.1 (b)]. Despite this, the current (i_g –) through passes through zero twice in a switching cycle [see Fig.1 (b)]. The thyristors of the switch can be easily turned off at these instants without causing any overvoltage. Similarly, while transitioning from CCM to DCM, the switch can be closed at any instant with zero current switching since the inductors $L_{b(dcm)}$ and carry the same instantaneous current ($i_g =$ during CCM.

It is shown that by simple on-off control of the switch S_A, we can realize two different power topologies [Fig. 1(a) and (b)] using a single converter system, while maintaining a constant switching frequency throughout. Now it is required to under-stand the various issues associated with turn-on and

turn-off instants of the switch S_A and to propose a suitable semiconductor switch for its realization.

Let us consider a case, when the converter system is required to be driven into DCM from its original CCM operation. This means that the switch S_A , which was originally off is now required to be closed. When the converter is operated under CCM, the inductors $L_{b(dcm)}$ and L_f carry the same instantaneous current $i_g = I_g$, while the filter capacitor C_f does not carry any current. Under this condition can be closed at any instant with zero current switching to drive the converter system into DCM.

The proposed controller works on the principle of resistor emulator as shown in Fig.3. One of the control objectives is to shape the averaged input I_g current follow the input voltage v_g as described in eqn.1 where R_e *i*s the desired input port resistance of the proposed converter.

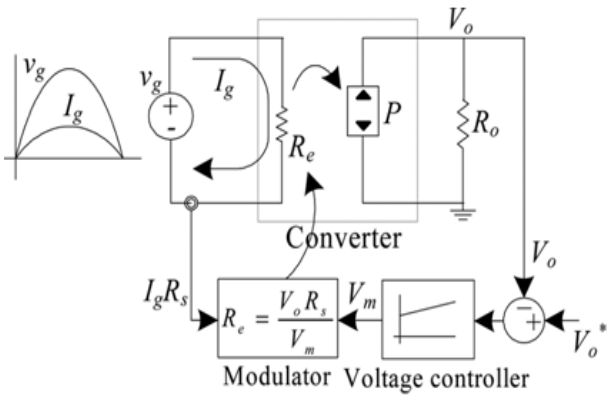

Fig.3: Resistor Emulator

$$I_g = {}^{v_g}/_{R_e} \qquad (1)$$

The next objective is to maintain the output voltage Vo at the desired reference level against all possible input voltage and load variations. This is achieved by regulating the input power to the converter through Re by closed loop control as shown in Fig.3. The output Vm of the voltage controller is used to regulate Re as shown in eqn. 2, where Rs is the gain in the current sensing path.

$$V_m = (V_o.R_s)/R_e \qquad (2)$$

Eqns.1, 2 and the quasi steady state approach are used to establish the necessary control equations for the DCM and CCM operations. A constant but high switching frequency $f_{sw} = 1/Ts$ is assumed throughout.

1) Control Equation for CCM: The converter is assumed to be operated in CCM with switch duty ratio D as shown in Fig. 1(b). The input voltage v_g may be related to the output voltage V_o and the duty ratio D as shown in (3). Equations (1)–(3) may be used to obtain the required control equation for CCM operation as shown in (4) - [7].

$$v_g = (1-D)V_o \quad (3)$$

$$I_g R_s = V_m - DV_m. \quad (4)$$

2) Control Equation for DCM: The converter is assumed to be operated in DCM as shown in Fig. 1(a). In each switching interval T_s the switch S is turned on for duration DT_s. The peak inductor current I_P and the switching-cycle averaged inductor current I_g can be expressed as in (5) and (6), respectively. Eliminating D_1 and I_P from (5) and (6), the expression for the switch duty ratio D is obtained as shown in (7) [5], [12]. The duty ratio D, shown in (7) depends on $I_g, L_{b(dcm)}, V_o, v_g$ & T_s . Equations (1), (2), and (7) are used to obtain the control equation for the DCM operation as shown in the following [12]:

$$I_P = \frac{v_g D T_S}{L_{b(dcm)}} = \frac{(V_o - v_g) D_1 T_S}{L_{b(dcm)}} \quad (5)$$

$$I_g = \frac{(D + D_1) I_P}{2} \quad (6)$$

$$D = \sqrt{\frac{2 I_g (V_o - v_g) L_{b(dcm)}}{V_o v_g T_S}} \quad (7)$$

$$I_g R_s = V_m - D^2 \left(\frac{R_s T_s}{2 L_{b(dcm)}} \right) V_o. \quad (8)$$

3) The Carrier Waves: The control equations (4) and (8) may be solved for D and accordingly the required gating pulses for the switch S under CCM and DCM operations may be generated. This, however, involves complex mathematic operations such as multiplications, divisions and square root operations, which increase the cost and complexity of controller. In order to avoid such complex operations a carrier-based approach is followed in this paper [4], [5], [12]. The right hand sides of (4) and (8) may be considered for the generation of two carriers $v_{c(ccm)}$ and $v_{c(dcm)}$ as shown in (9) and (10),

respectively, where D is replaced by t/T_s [4], [5]. The carriers (9) and (10) represent linear and non linear carriers for CCM and DCM operations, respectively

$$v_{c(ccm)}(t) = V_m - \left(\frac{V_m}{T_s}\right) t; \quad 0 < t < T \qquad (9)$$

$$v_{c(dcm)}(t) = V_m - \left(\frac{R_s V_o}{2L_{b(dcm)} T_s}\right) t^2; \quad 0 < t < T. \qquad (10)$$

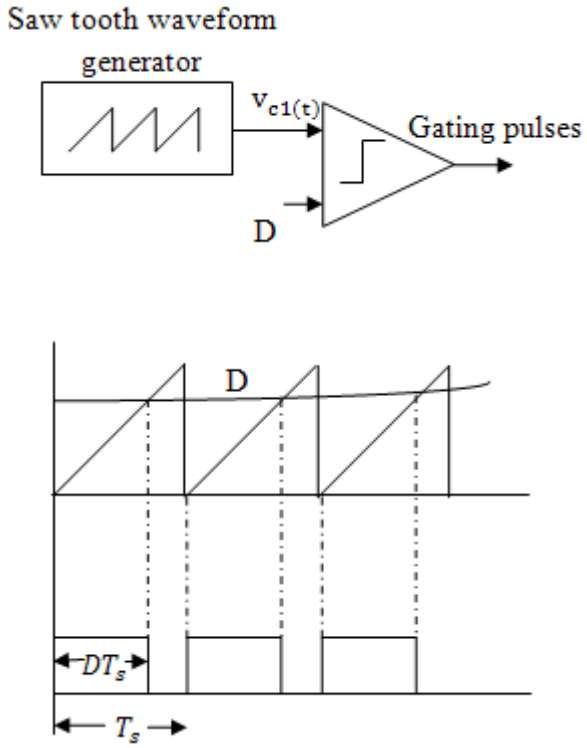

Fig 3(a) First method for producing gate pulses

4) Gating Pulse Generation under DCM and CCM: The process of gate pulse generation under DCM and CCM operations are shown in Fig. 4(a) and (b), respectively. The carriers $v_{c(dcm)}$ and $v_{c(ccm)}$ can be generated using simple op-amp based integrator and amplifier circuits as shown. The integrators are reset at the beginning of each switching cycle by a constant-frequency clock of negligible pulse width. At the

beginning of each switching cycle$(t=0)$, each of the above carriers start from the same initial valueV_m. At $t = DT_s$, the carrier $v_{c(dcm)}$equals the RHS of (4), while the carrier $v_{c(ccm)}$equals the RHS of (8). Further, at$t = DT_s$, the RHS of (9) and that of (10) equal the measured input currentI_gR_s [see (4) and (8)]. Thus, the required gating pulses for the switch can be generated by comparing the measured input currentI_gR_s with either of the above carriers in a comparator. The linear carrier (9) may be used during CCM, while the nonlinear carrier (10) may be selected during DCM.

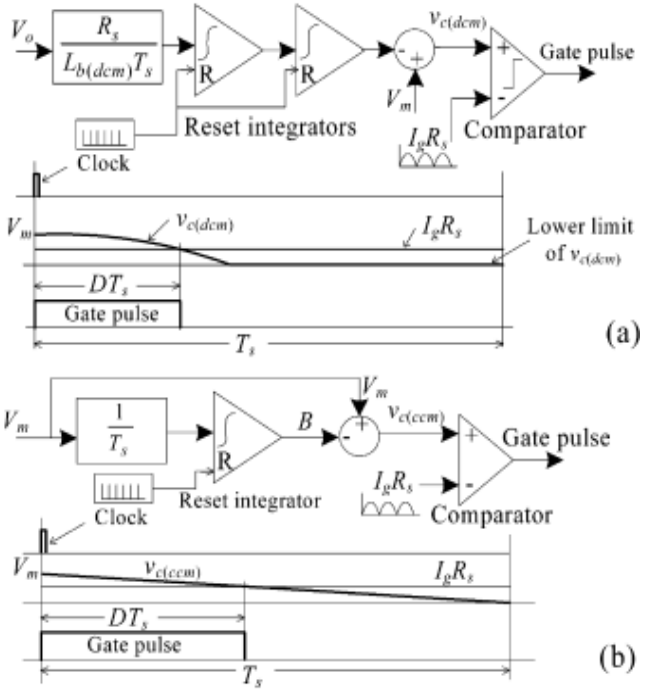

Fig4: Gating pulse generation under (a) DCM and (b) CCM.

The converter system is required to be operated in DCM during lighter load and in CCM for higher load. The measured load currentI_oR_s may be compared with a reference load current $I_{o(\mathrm{ref})}$ [set at a level corresponding to the load boundary between CCM and DCM operations (discussed in Section III)] in a hysteresis comparator to select the desired operating mode (CCM or DCM). It can be seen that the process of gating pulse generation under CCM is different from the process under DCM. Further, the DCM operation is effective only during lighter loads, while the CCM is during higher loads. A one-to-one comparison of the carriers and the duty ratios under CCM and DCM for an output power of 300 W is

given below.

5) Comparison of the Carriers and the Duty Ratios: Let us define the voltage ratio m_g as shown in (11), where ω is the supply angular frequency, v_g and V_{gm} are the instantaneous and the peak input voltages, respectively, and $M_g = V_{gm}/V_o$

$$m_g = \frac{v_g}{V_o} = \frac{V_{gm}\sin(\omega t)}{V_o} = M_g \sin(\omega t). \qquad (11)$$

Equations (1) and (11) may be used to modify (3) and (7) as

in (12) and (13), respectively, where $K = 2L_{b(dcm)}f_{sw}/R_e$ .It can be seen that the duty ratio under CCM depends only on m_g .However, in addition to m_g, the duty ratio under DCM depends on the output power through parameter K

$$D_{(ccm)} = 1 - \frac{v_g}{V_o} = (1 - m_g) \qquad (12)$$

$$D_{(dcm)} = \sqrt{K(1 - m_g)}. \qquad (13)$$

The variations of the carriers (9) and (10) in a particular switching cycle T_s are shown in Fig. 5(a). The variations of $D_{(ccm)}$ and $D_{(dcm)}$ over a half fundamental cycle are shown in Fig. 5(b). The output power in all the above cases is 300 W (see parameters in Section III-G).

(6)Load Current Feed forward: *The voltage loop of the pro-posed converter system is required to be designed for low band-width (see Section III-F) to limit the input current distortion caused by the output voltage ripple [5]. This results in poor system dynamic response with significant undershoot and over-shoot in the output voltage V_o during sudden changes in the load. A typical settling time of the voltage loop for a step change in load is reported to be around 250 ms [5]. A simple load cur-rent feed forward scheme is used in this paper to improve the dynamic response of the converter system and also to ensure a smooth transition from one operating mode to the other. It can be seen from (2) that the output V_m of the voltage controller controls the input power to the converter throughR_e. However, the output power of the converter is controlled by the load currentI_o. At steady state, the input power equals the output power (internal losses are neglected) as shown in (14). Equation (14) may be used to express the steady state value V_m of in terms of I_o as shown in*

$$P_o = V_o I_o = \frac{V_o^2}{R_o} = \frac{V_{gm} I_{gm}}{2} = \frac{V_{gm}^2}{2R_e} \qquad (14)$$

$$V_m = \left(\frac{2R_s V_o^2}{V_{gm}^2}\right) I_o = \left(\frac{2R_s}{M_g^2}\right) I_o. \qquad (15)$$

Though the steady state value of is V_m proportional to I_o, it is not so during transients. When the load changes suddenly, the voltage loop acts slowly to adjust V_m from its original value to a new steady state value depending on its bandwidth. During this time, the input-output power balance gets disturbed. This appears as overshoot or undershoot in the output voltage V_o.

In order to avoid this issue, the control parameter V_m is reconstituted from two control inputs as shown in (16).

$$V_m = V_{m(VC)} + V_{m(FF)} = V_{m(VC)} + \left(2/M_g^2\right) I_o R_s. \quad (16)$$

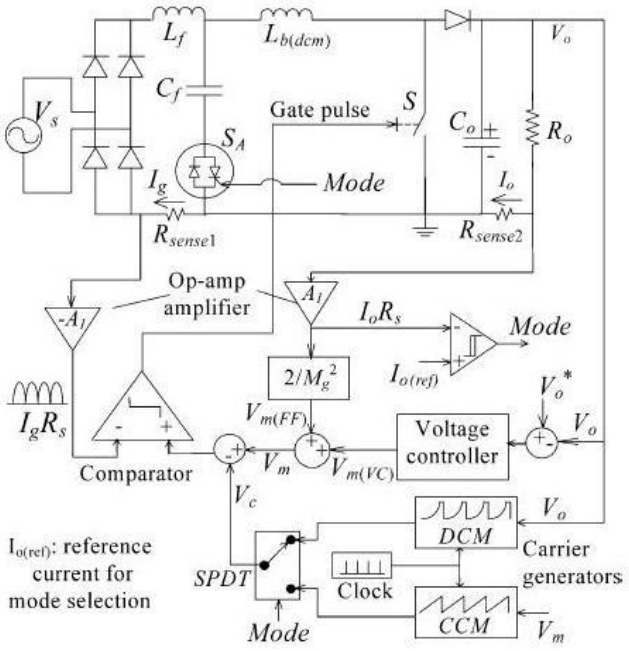

Fig 5: Proposed Controller

The feed forward input $V_{m(FF)}$ helps the control parameter V_m settle immediately to the neighborhood of its final value during above transients. The fine adjustment of V_m is performed slowly through $V_{m(VC)}$. The rated value of M_g may be used to derive the feed forward input $V_{m(FF)}$. It can be

shown that at rated input voltage, $V_{m(VC)}$ is zero. However, the output $V_{m(VC)}$ takes a non-zero value, when the input voltage deviates from its rated value.

The complete block diagram of the proposed control scheme is shown in Fig.5. All measurements can be performed with respect to the negative terminal of the output capacitor C_o. It can be seen that no electrical isolation is required for the measurements as well as for gate drive.

III. DESIGN & ANALYSIS OF BOOST RECTIFIER

This section explains a detailed design method for selecting different passive components such as $L_{b(dcm)}$, L_f, C_f and C_o and the parameters of the voltage controller.

A. Load Boundary between CCM and DCM Operations

For the same output power, the peak device current in DCM is much higher than in CCM. Therefore, it is required to set the load boundary between CCM and DCM operations to a level, where the maximum device current $I_{P(dcm)}$ under DCM is less than or equal to the rated device current under CCM.

Equations (5), (7), and (14) may be used to express the peak device current under DCM as in (17), where is de-fined in (18), $I_g = I_{gm}\sin(\omega t)$ and $P_{o(dcm(max))}$ is the desired maximum output power under DCM. Equation (17) has a maximum value $I_{P(dcm(max))}$ at $\omega t = \sin^{-1}[2/(3M_g)]$ as in

$$I_{P(\mathrm{dcm})} = K_1 m_g \sqrt{(1 - m_g)} \qquad (17)$$

$$K_1 = \frac{2}{M_g}\sqrt{\frac{P_{o(\mathrm{dcm(max)})}}{L_{b(\mathrm{dcm})} f_{sw}}} \qquad (18)$$

$$I_{P(\mathrm{dcm(max)})} = \left(\frac{2}{3\sqrt{3}}\right) K_1. \qquad (19)$$

Using (14), the peak device current $I_{P(\mathrm{ccm(max)})}$ under CCM is shown in (20), where $P_{o(\mathrm{ccm(max)})}$ is the maximum output power under CCM, which decides the current rating of the device. It should be noted that in (20) the effect of ripple current in the inductor has been neglected. In order to keep the peak de-vice current under DCM within $I_{P(\mathrm{ccm(max)})}$, we have the constraints

$$I_{P(\text{ccm}(\max))} = \frac{2P_{o(\text{ccm}(\max))}}{V_{gm}} \quad (20)$$

$$I_{P(\text{dcm}(\max))} \leq I_{P(\text{ccm}(\max))} \quad (21)$$

$$P_{o(\text{dcm}(\max))} \leq \left(\frac{27L_{b(\text{dcm})}f_{sw}}{4V_o^2}\right) P^2_{o(\text{ccm}(\max))}. \quad (22)$$

It is seen in (22) that for a given V_o, f_{sw} and $P_{o(\text{ccm}(\max))}$ the selection of the load boundary between CCM and DCM operations depends on $L_{b(\text{dcm})}$.

B. ***Boost Inductor*** $L_{b(\text{dcm})}$

In Fig. 1(a), the interval D_2T_s becomes zero, when the converter operates at CCM–DCM boundary (note that the CCM–DCM boundary is different from the load boundary between CCM and DCM operations). The corresponding average inductor current I_g is shown in (23). Equations (1) and (23) are used to obtain the corresponding duty ratio as in

$$I_g = \frac{I_P}{2} = \frac{v_g D T_s}{2L_{b(\text{dcm})}} \quad (23)$$

$$D_{(\text{ccm}-\text{dcm})} = K = \frac{2L_{b(\text{dcm})}f_{sw}}{R_e}. \quad (24)$$

Using (13) and (24), the condition for operation at CCM-DCM boundary is shown in (25). The RHS of (25) has a minimum value of $(1 - M_g)$ at the peak of the input voltage $(m_g = M_g)$. The inductor $L_{b(\text{dcm})}$ is selected such a way that for an output power $P_{o(\text{dcm}(\max))}$, the operation of the converter is on the CCM–DCM boundary at the peak of the input voltage in a half line cycle as in (26). Equations (22) and (26) are used to determine the load boundary between CCM and DCM operations as in (27)

$$K = (1 - m_g) \quad (25)$$

$$L_{b(\text{dcm})} = \frac{(1 - M_g)V_{gm}^2}{4P_{o(\text{dcm}(max))}f_{sw}} \quad (26)$$

$$P_{o(\text{dcm}(\max))} = \left(\frac{3\sqrt{3}M_g\sqrt{(1-M_g)}}{4}\right) P_{o(\text{ccm}(\max))}. \quad (27)$$

C. ***Boost Inductor*** $L_{b(\text{ccm})}$

Under CCM [Fig. 1(b)], the peak-to-peak ripple ΔI_g in the inductor current i_q as a per unit of the peak averaged inductor current I_{gm} is shown in (28), where $D_{(\text{ccm})}$ is defined in (12).

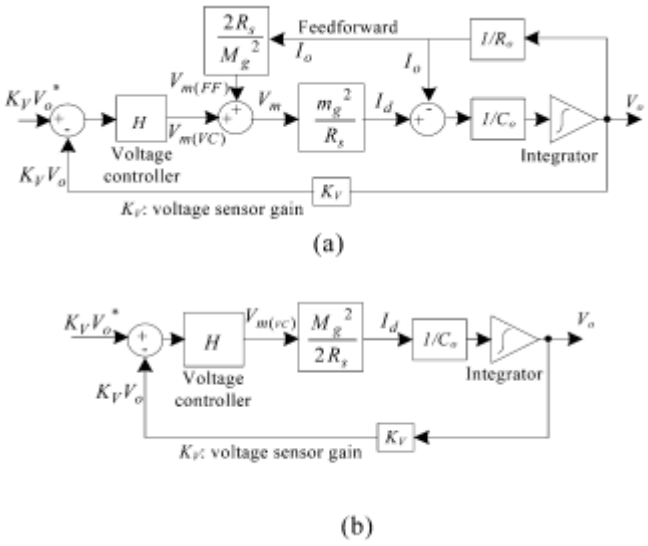

Fig6: (a) Averaged model of the converter & (b) voltage loop

The value of $L_{b(\text{ccm})}$ is selected based on the maximum value of $\Delta I_g/I_{gm}$ at minimum output power under CCM as in (29), which occurs at $\omega t = \sin^{-1}(0.5/M_g)$.

$$\frac{\Delta I_g}{I_{gm}} = \frac{v_g D_{(\text{ccm})} T_s}{L_{b(\text{ccm})} I_{gm}} = \left(\frac{M_g V_o^2}{2L_{b(\text{ccm})} f_{sw} P_o}\right) m_g(1 - m_g) \qquad (28)$$

$$L_{b(\text{ccm})} = \frac{M_g V_o^2}{8P_{o(\text{dcm(max)})} f_{sw} (\Delta I_{g\max}/I_{gm})}. \qquad (29)$$

D. ***Input Filter*** L_f *and* C_f

The value of $L_f = L_{b(\text{ccm})} - L_{b(\text{dcm})}$ can be obtained from (26) and (29). The parameter C_f may be

expressed in terms of L_f and the filter corner frequency f_c as in (30), where $n = f_{sw}/f_c$. The value of C_f may be obtained by selecting a suitable value for n. A detailed design procedure is given in [13].

$$C_f = \frac{1}{L_f(2\pi f_c)^2} \approx \frac{0.025n^2}{L_f f_{sw}^2}. \quad (30)$$

E. ***DC Bus Capacitor*** C_o

The capacitor C_o (Fig. 2) carries low frequency as well as high frequency current components. For selecting the value of C_o , the high frequency current components may be neglected. The low frequency current components may be obtained from the switching-cycle averaged capacitor current I_C as in (31), where I_d is the averaged diode current, shown in (32) and $I_a = I_{gm}\sin(\omega t)$. It can be shown that (32) is valid for both CCM and DCM

$$I_C = I_d - I_o = -I_o.\cos(2\omega t) \quad (31)$$
$$I_d = m_g I_g. \quad (32)$$

The peak-to-peak ripple ΔV_o in V_o is shown in (33). Using (14) and (33), the capacitor C_o is designed for the maximum possible peak-to-peak ripple $\Delta V_{o(max)}$ as in (34), where f is the fundamental frequency.

$$\Delta V_o = \frac{1}{\omega C_o}\int_{\pi/4}^{3\pi/4} I_c d\omega t = \frac{I_o}{\omega C_o} \quad (33)$$
$$C_o = \frac{P_{o(\text{ccm(max)})}}{2\pi f V_o^2\left(\Delta V_{o(max)}/V_o\right)}. \quad (34)$$

F. ***Voltage Loop***

Equations (1), (2), and (11) may be used to modify (32) as in (35). It can be seen from (35) that I_d has a dc component and an ac component. The dc component of I_d equals the load $I_o$current, while its ac component causes the voltage ripple $\tilde{v}_o$ in V_c as in

$$I_d = \left(\frac{m_g^2}{R_s}\right) V_m = \left(\frac{M_g^2}{2R_s}\right) V_m - \left(\frac{M_g^2 V_m}{2R_s}\right) \cos(2\omega t) \quad (35)$$

$$\tilde{v}_o = \frac{1}{\omega C_o} \int I_{d(ac)} d\omega t = \left(\frac{-V_o}{2\omega C_o R_o}\right) \sin(2\omega t). \quad (36)$$

The averaged model of the converter system, including the load current feed forward scheme, is shown in Fig. 7(a). The Feed forward scheme makes the voltage loop insensitive to load current as seen in Fig. 7(b).

A simple PI type voltage controller, shown in (37), is used to control the above system. Equation (38) shows the steady state output $V_{m(VC)}$ of the voltage controller. At steady state, the dc component of the output voltage V_o equals the reference voltage V_o^* , while its ripple component (36) is processed by the voltage controller as in (39). The parameters K_{PI} and T_{PI} of the voltage controller are selected in such a way that the voltage loop does not respond to the dc bus voltage ripple [5]. Compared to the proportional term, the effect of the integral term in (39) may be ignored, when the zero of the voltage controller is placed well below the twice-line frequency 2f (i.e., 100 Hz) [5]

$$H(s) = \frac{K_{PI}(1 + sT_{PI})}{sT_{PI}} \quad (37)$$

$$V_{m(VC)} = K_{PI}K_V (V_o^* - V_o) + \frac{K_{PI}K_V}{T_{PI}} \int (V_o^* - V_o)\, dt \quad (38)$$

$$\tilde{v}_{m(VC)} = -K_{PI}K_V \tilde{v}_o - \frac{K_{PI}K_V}{T_{PI}} \int \tilde{v}_o dt \approx -K_{PI}K_V \tilde{v}_o. \quad (39)$$

An ideal condition is when there is no ripple in V_o and V_m. Equations (1) and (2) may be used to express the steady state input current I_g as in (40). Now, considering the ripple in V_o and in V_m , the steady

state input current (40) is modified as in (41), whose parameters are shown in

$$I_g = \frac{V_m v_g}{V_o R_s} \tag{40}$$

$$I_g = \frac{v_g}{R_e}\left(\frac{1 - A(\tilde{v}_o/V_o)}{1 + (\tilde{v}_o/V_o)}\right) \approx \frac{v_g}{R_e}[1 + AB\sin(2\omega t)]$$
$$= I_{gm}[\sin(\omega t) + I_2\cos(\omega t) - I_2\cos(3\omega t)] \tag{41}$$
$$A = \frac{K_{PI}K_V R_e}{R_s}; \quad B = \frac{1}{2\omega C_o R_o}; \quad \frac{\tilde{v}_o}{V_o} \ll 1;$$
$$I_{gm} = \frac{V_{gm}}{R_e}; \quad I_2 = \frac{AB}{2}. \tag{42}$$

It can be seen from (41) that in absence of output voltage ripple, the average inductor current I_g equals the desired current v_g/R_e. .However, the presence of ripple in V_o introduces an un-wanted displacement term $I_{gm}I_2\cos(\omega t)$ and a third-harmonic distortion term $I_{gm}I_2\cos(3\omega t)$ in I_g. Both of these could be controlled through K_{PI} . A low valued K_{PI} is required to maintain a low input current distortion and displacement. However, a high valued K_{PI} is required for good voltage loop response. Hence, there is a tradeoff between the fastness of response and quality of input current.

IV. SIMULATION AND EXPERIMENTAL RESULTS

1) Parameters of boost converter

The single phase CCM-DCM boost rectifier is implemented using Matlab/Simulink toolbox. The specifications used for the simulation are as follows

Table 1: **Parameters of boost converter**

Rated input voltage :	110 V (rms)
Rated output voltage :	215 V
Line frequency :	50 Hz
Switching frequency:	10 kHz
Rated output power:	600 W

Maximum output power $P_{o(ccm)(ma}$:	660 W (110% rated)
Max p-to-p ripple in the output voltage: $\Delta \ V_{o(max)} = 0.04 *$ Vo	8.6 V
$\Delta I_{g(max)} = 0.2 * I_{gm}$ Max p-to-p ripple in the i/p current (Under CCM)	0.6 A
Current sensing gain R_s	0.5 Ω
Maximum output power $P_{o(dcm)(max)}$	330 W
Boost inductor $L_{b(dcm)}$	500 µH
Filter inductance L_f	6 mH
Filter capacitor C_f	4 µH
Output capacitor C_o	1100 µF

2) **Simulink model of CCM-DCM boost rectifier**

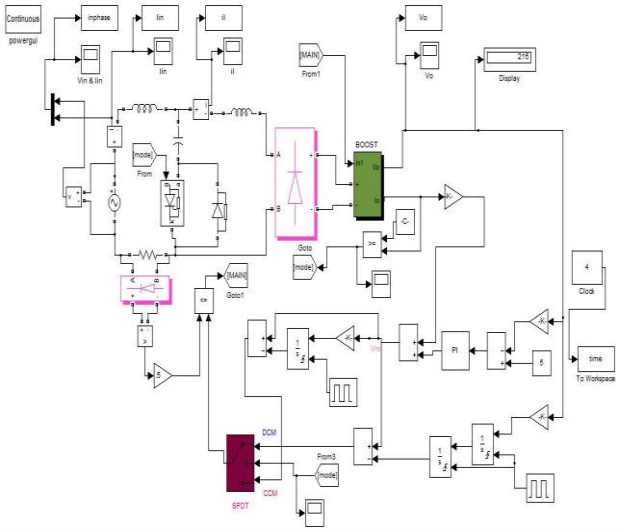

Fig 7: Simulink model for the proposed system

3)**Simulink model of conventional CCM-DCM boost rectifier**

4)

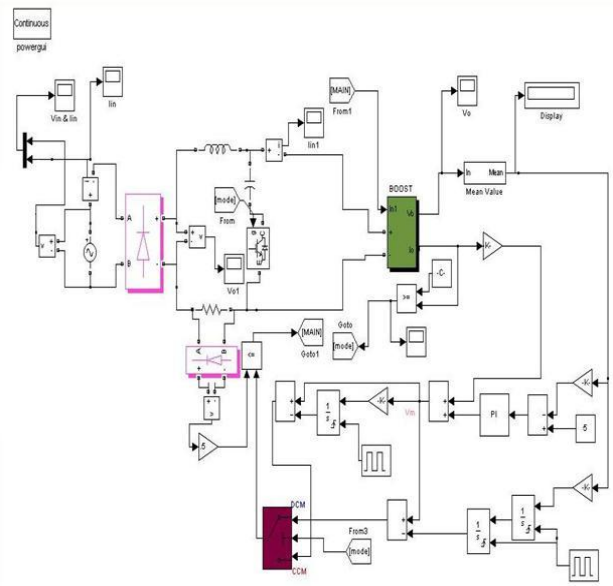

Fig 8: Simulink model for the conventional system

For rated power and rated input voltage the following are the simulation results. Figs. 9,10,11,12 and 13 shows the transient response of output voltage, output current, input current and input voltage, input current, and current through the inductor for step change in load without feed forward loop. From Fig. 5.4 we can observe that the settling time of the voltage loop for a step change in load is around 250 msec

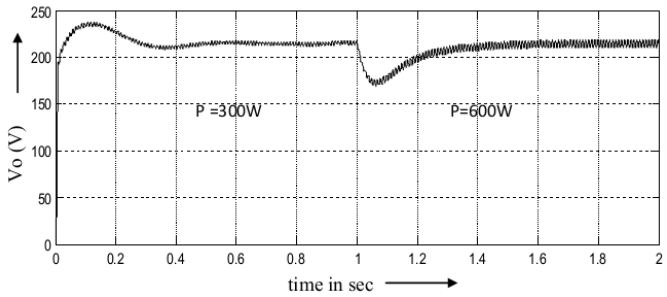

Fig.9: Simulation waveform of o/p voltage without load current feed forward loop

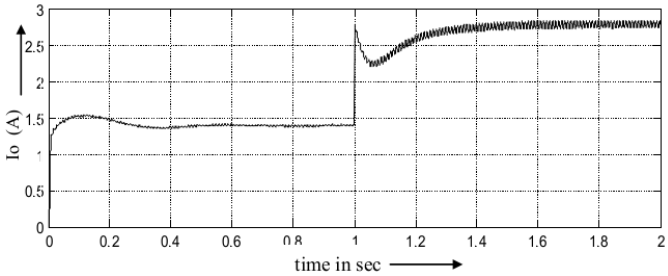

Fig.10: Simulation waveform of o/p current without load current feed forward loop

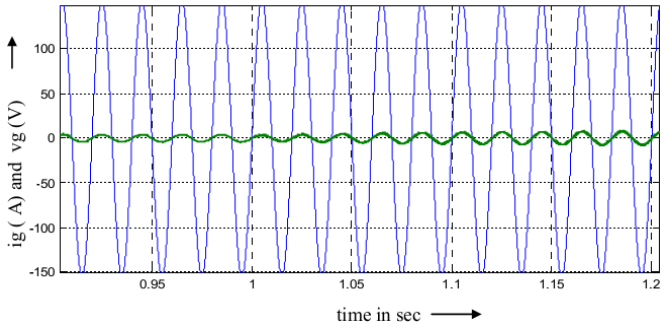

Fig.11: i/p voltage and i/p current waveform without load current feed forward loop

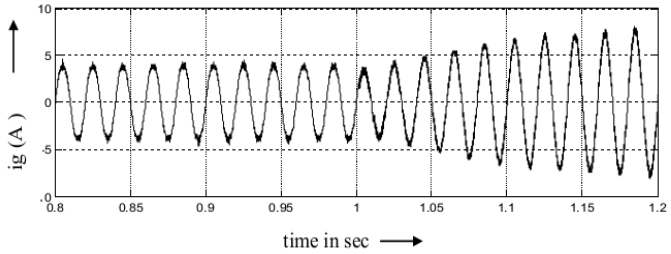

Fig.12: Input current waveform without load current feed forward loop

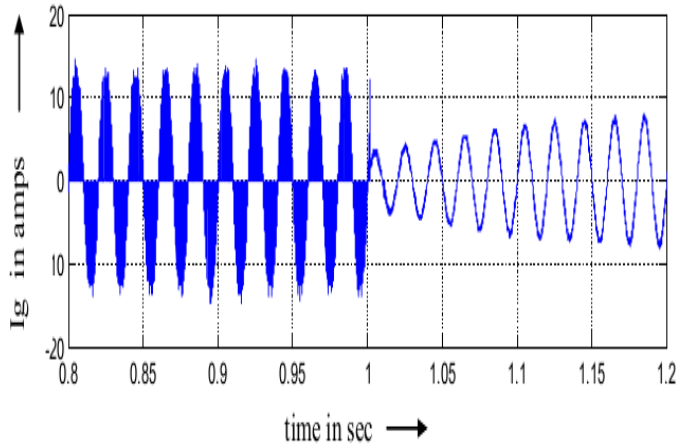

Fig.13: Current through Lb (dcm) waveform without load current feed forward loop

From the simulation it is observed that the settling time of the voltage loop is reduced when feed forward loop is applied. In case of without feed forward loop the settling time is 250 msec. From the Fig.14 the output voltage is having very less undershoot as compared to the system without feed forward loop at the point where the load changes.

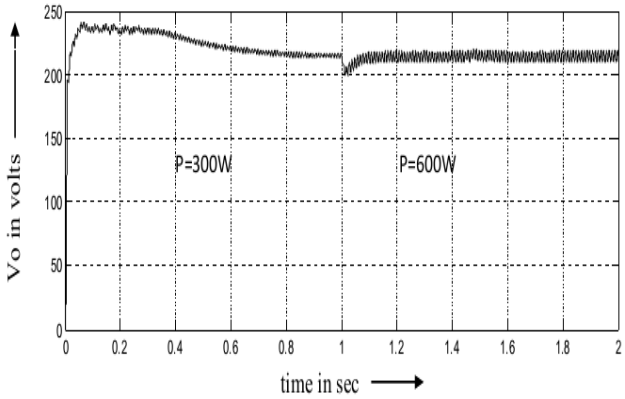

Fig.14: Output voltage waveform with load current feed forward loop

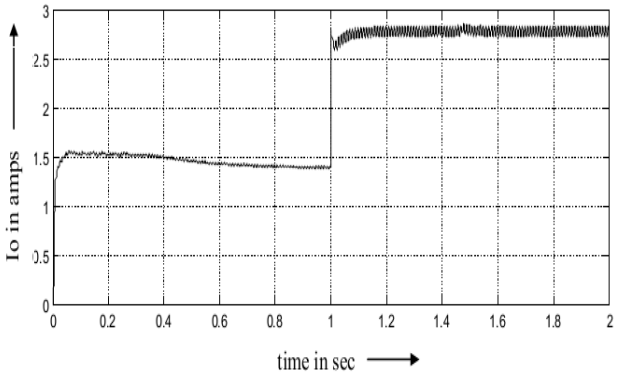

Fig.15: Output current waveform with load current feed forward loop

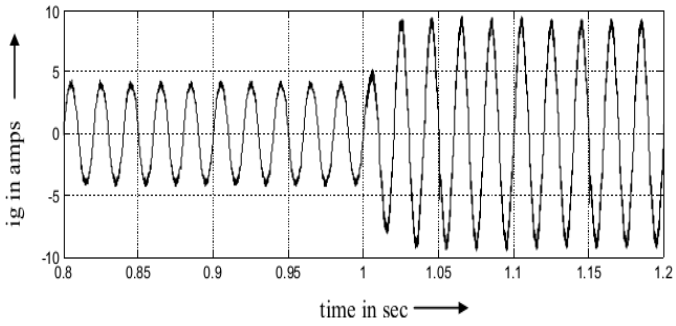

Fig.16: Input current waveform with load current feed forward loop

The steady state input voltage and input current waveforms, corresponding to 300W and 600Woutput power are shown in Fig.11 and 16. The converter is operated in DCM, where the auxiliary switch is turned on and the nonlinear carrier is selected. The input voltage and the current through the boost inductor are shown in Fig.13. Fig.19 and 18 shows the %THD of the input current, which is about less than 5%.

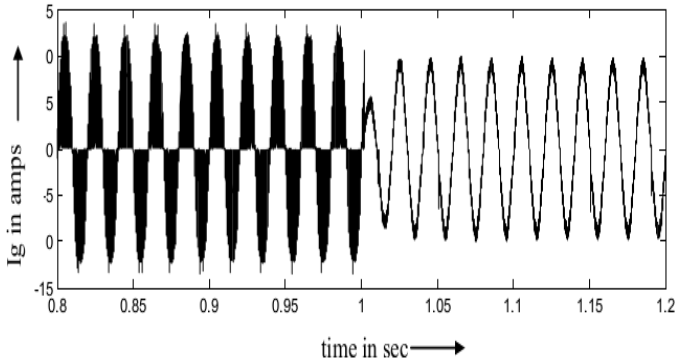

Fig. 17 Current through Lb (dcm) waveform with load current feed forward loop

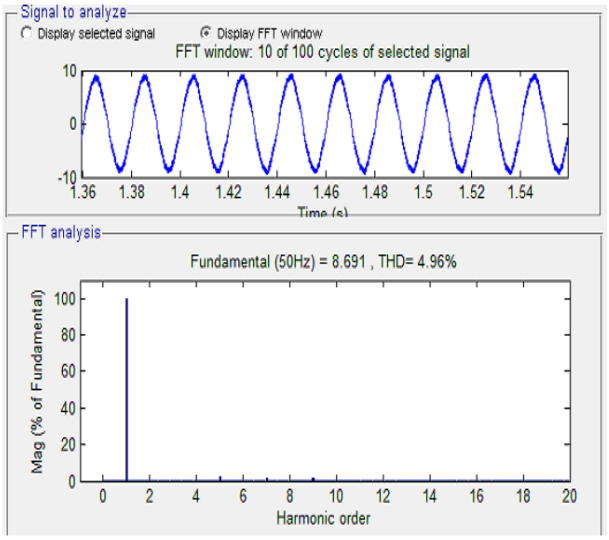

Fig.18: Input current THD for CCM

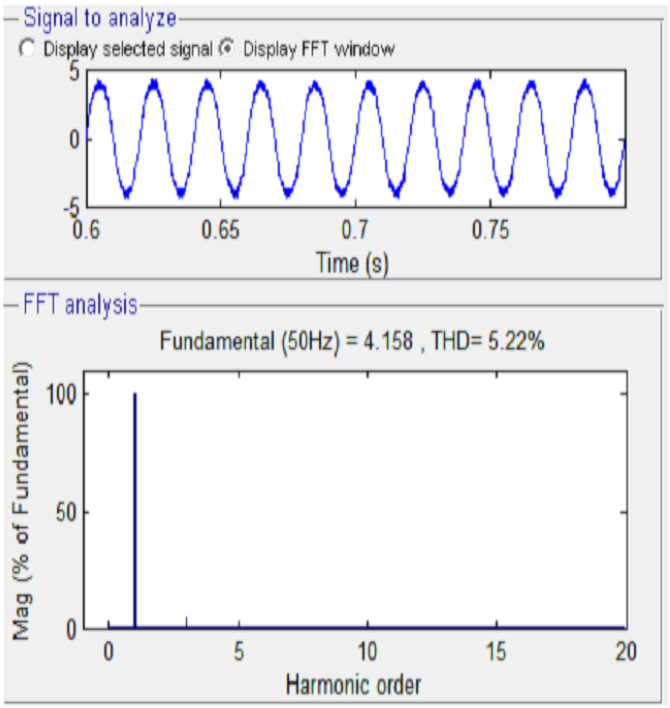

Fig.19: Input current THD for DCM

V. CONCLUSION

Pulse width modulation rectifiers are extensively used in battery charger, regulated dc voltage source, UPS systems, static frequency changer and ac line conditioner, where the main requirements are unidirectional power flow, regulated output dc voltage and near unity input power factor. In case of single switch boost rectifier, additional requirement of dc bus voltage balancing is essential. The conventional control techniques involve complex mathematical operations, which increase the cost and complexity of the controller. Simple control schemes based on constant-switching-frequency resistance emulation control, which do not require any of the above operations, are developed in this thesis work for PWM boost rectifier.

The power circuit of the proposed converter can be configured either for DCM or for CCM by simple on–off control of an auxiliary switch. Similarly, the proposed control circuit can also be configured either for CCM or for DCM simply by choosing the appropriate carriers (a linear carrier for

CCM and a nonlinear carrier for DCM). The measured load current is used to select the desired operating mode. The required switching instants are generated by comparing the measured input current with one of the above carriers in a modulator without using any multiplication, division, square root operation, and input voltage sensing.

All the necessary design equations are provided to select the passive components. The averaged model of the proposed rectifier system is presented. Using such model, a design guideline for selecting the parameters of the voltage controller is presented. A simple load current feed forward scheme is presented to improve the dynamic response of the system against sudden change in loads.

VI. REFERENCES

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