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CMOS DESIGN OF TREE MULTIPLIER USING LOW POWER AND AREA EFFICIENT FULL ADDER

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Abstract:-Digital electronic computations started with the introduction of vacuum tubes. But implementation of larger engines became economically and practically infeasible. The invention of the transistor, followed by the introduction of the bipolar transistor led to the first successful IC logic family, TTL (Transistor-Transistor Logic). Next was the turn of the MOS digital integrated circuit approach. As electrons have higher mobility than holes, NMOS was preferred later so processors used NMOS-only logic, with higher speed relative to the PMOS logic. But later, NMOS-only logic started suffering from the same problem: power consumption. Finally the balance tilted towards the CMOS technology.

In case of CMOS, addition of a single input increases the device count by 2 and thus increases the propagation delay. New logic styles were developed to minimise the propagation delay and chip area. We present high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP).

Wallace high-speed multipliers use full adders and half adders in their reduction phase. Half adders do not reduce the number of partial product bits. Therefore, minimizing the number of half adders used in a multiplier reduction will reduce the complexity. A modification to the Wallace reduction is presented that ensures that the delay is the same as for the conventional Wallace reduction. The modified reduction method greatly reduces the number of half adders; producing implementations with 80 percent fewer half adders than standard Wallace multipliers, with a very slight increase in the number of full adders.

Keywords: Complementary metal oxide semiconductor (CMOS), Power delay product (PDP), Transistor transistor logic (TTL), Carry save adder (CSA) , Compound domino logic (CDL), Complementary pass-transistor logic (CPL), Differential cascode voltage switch (DCVS), Double pass-transistor logic (DPL), Swing restored CPL (SR-CPL).

1.INTRODUCTION

Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios.

We done the design and performance comparison of full-adder cells implemented with an alternative internal logic structure, based on the obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption.

Used this adder designed as a carry save adder for well-known Wallace high-speed multiplier to reduce an N-row bit product matrix to an equivalent two row matrix that is then summed with a carry propagating adder to give

the product. It is a fully parallel version of the multiplier used in the IBM Stretch computer. The carry save adders are conventional full adders whose carries are not connected, so that three words are taken in and two words are output. the Wallace multiplier also uses half adders in the reduction phase. This modified design that greatly reduces the number of half adders in Wallace tree multipliers.

2. PREVIOUS FULL-ADDER OPTIMIZATIONS

Many concepts have been arrived regarding the optimization of low-power full-adders,trying different options for the logic style (standard CMOS, differential cascode voltage switch (DCVS),complementary pass-transistor logic (CPL),double pass-transistor logic (DPL),swing restored CPL (SR-CPL),and hybrid styles, and the logic structure used to build the adder module .

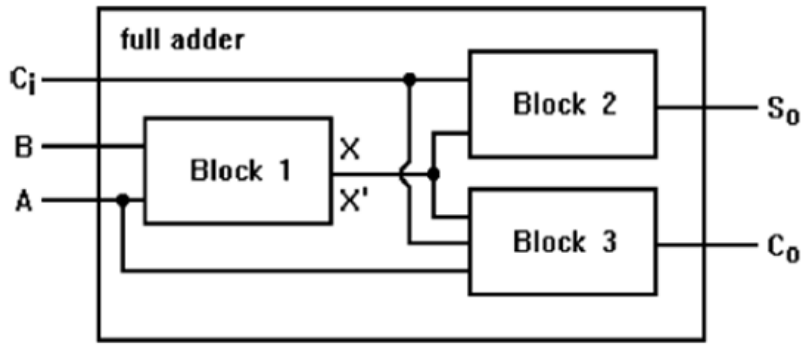

Fig.1 Full-adder cell formed by three main logical blocks.

The internal logic structure shown in Fig.1 has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain A xor B and A xnor B (Block 1), and XOR blocks or multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3). A deep comparative study to determine the best implementation for Block 1was presented in [5], and an important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig.1, is that it is necessary to obtain an intermediate signal A XOR B and its complement, which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full adder depend on the delay and voltage swing of the A XOR B signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

3. WALLACE TREE

Wallace trees are irregular in the sense that the informal description does not specify a systematic method for the compressor interconnections. However, it is an efficient implementation of adding partial products in parallel. The Wallace tree operates in three steps:

1. Multiply: Each bit of multiplicand is ANDed with each bit of multiplier yielding n2 results. Depending on the position of the multiplied bits, the wires carry different weights, for example, wire of bit a2b3 weighs 32.
2. Addition: As long as there are more than 3 wires with the same weights add a following layer. Take 3 wires of same weight and input them into a full adder. The result will be an output wire of 32 same weight. If there are two wires of same weight, add them using half-adder and if only one is left, connect it to the next layer.
3. Group the wires in two numbers and add in a conventional adder. Wallace tree has been used during the design of multipliers for this thesis. A typical Wallace tree architecture is shown in Figure 2.

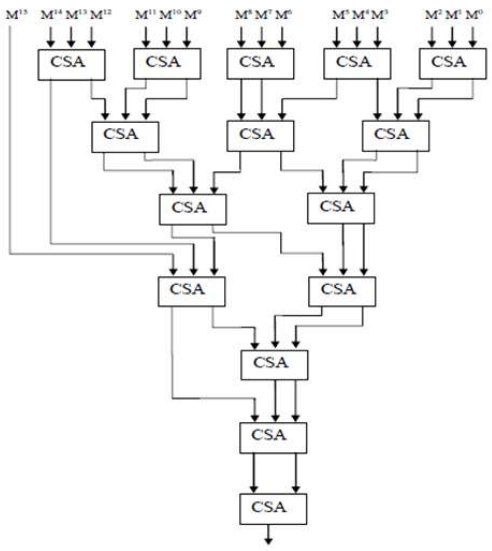

Figure 2: Typical Wallace tree

3.1 Previous approach of wallace reduction

For the conventional Wallace reduction method, once the partial product array (of N2 bits) is formed, adjacent rows are collected into non overlapping groups of three. Each group of three rows is reduced by

1) applying a full adder to each column that contains three bits.
2) applying a half adder to each column that contains two bits.
3) passing any single bit columns to the next stage without processing.

This reduction method is applied to each successive stage until only two rows remain. The final two rows are summed with a carry propagating adder. This process is illustrated by the conventional 9-bit by 9-bit Wallace multiplier shown in Fig. 3. Light lines show the three row groupings. The reduction is performed in four stages (each with the delay of one full adder) with a total of 50 full adders and 21 half adders. The third phase will require a 13-bit wide adder.

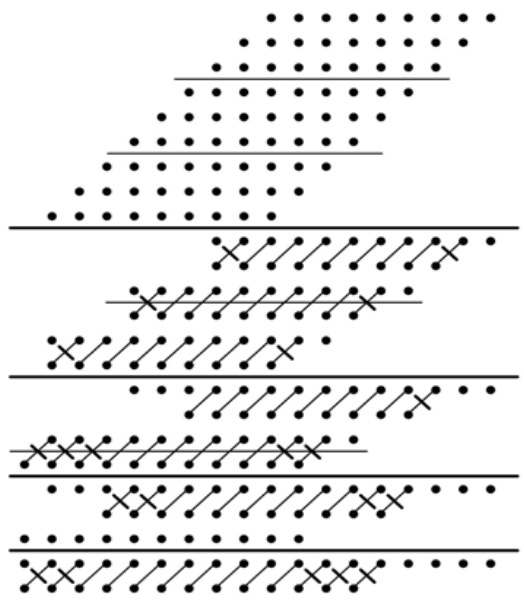

Fig.3 Conventional Wallace 9-bit by 9-bit reduction.

4. ALTERNATIVE LOGIC STRUCTURE FOR A FULL-ADDER

Examining the full-adder's true-table in Table I, it can be seen that the So output is equal to the A? B value when C=0 and it is equal t (A ? B)bar when C=1. Thus, a multiplexer can be used to obtain the respective value taking the_ input as the selection signal. Following the same criteria, the Co output is equal to the A.B value when C=0, and it is equal to A+B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A? B and (A? B)bar signals, another block to obtain the A.B and A+B signals, and two multiplexers being driven by the C input to generate the So and Co outputs, as shown in Fig. 4 .

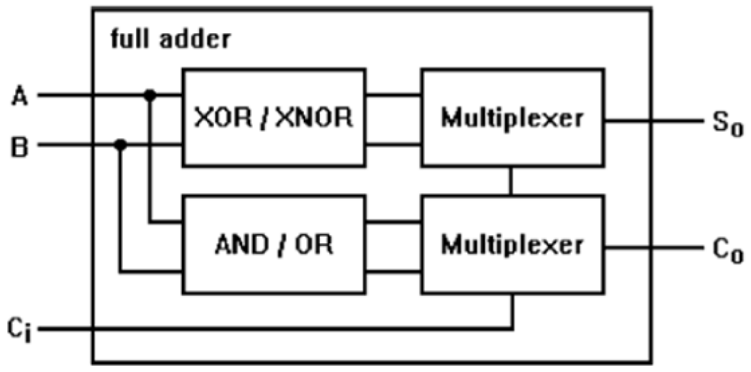

Fig 4 Alternative logic scheme for designing full-adder cells

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(True-table fir a I bit full adder, A,B and C are inputs S0 and C0 are outputs)

multiplexers being driven by the C input to generate the So and Co outputs, as shown in Fig. 4.The features and advantages of this logic structure are as follows.

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.
• The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced.
• The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.
• The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

4.1 Modified adder design (Gate level)

Based on the previous adder design analysis two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig.5 . Fig.6 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output. In Fig.5, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the Co output.

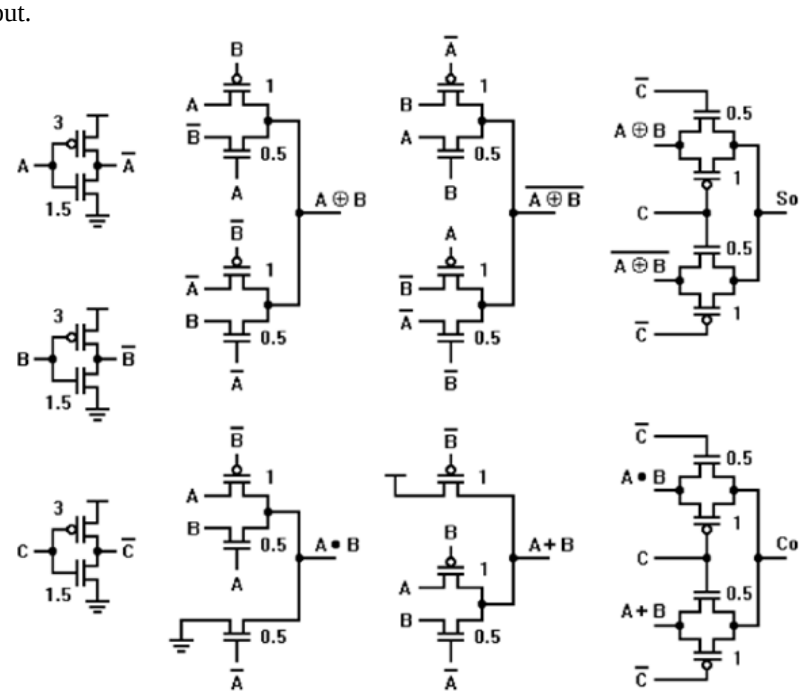

Fig. 5. Full-adder designed with the proposed logic structure and a DPL logic Style

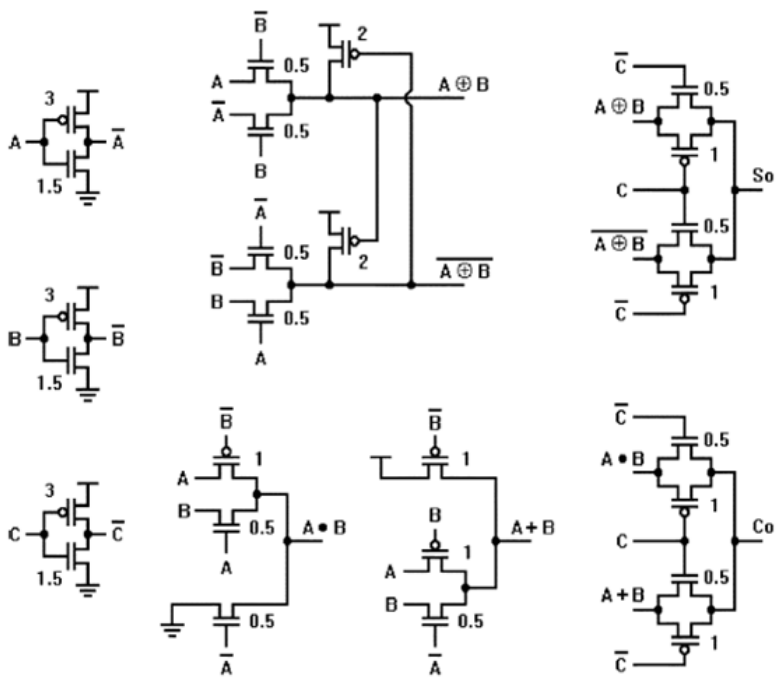

Fig. 6 Full-adder designed with the proposed logic

structure and a SR-CPL logic style at the outputs. The size of the input buffers lets to experience some degradation in the input signals, and the size of the output buffers equals the load of four small inverters for this technology. This test bed is presented as a generalization of statics CMOS gates driving and been driven for the full-adder cell under test. The main advantage of using this simulation environment is that the following power components are taken into account, in addition to the dynamic one.

5. MODIFIED WALLACE REDUCTION

This section presents the modified Wallace method for reducing the partial product array (the second phase). As shown in Fig. 7, the initial partial product array of the first phase is changed by shifting bits in the left half of the array upward to form an inverted pyramid array (the partial product generation method is the same, no data are changed; only their vertical position is shifted).

In the second phase, the modified Wallace approach is similar to the conventional Wallace approach in that it uses as many full adders as possible, but different in that it only uses half adders when necessary to ensure that the number of reduction stages is the same as for a conventional Wallace multiplier.

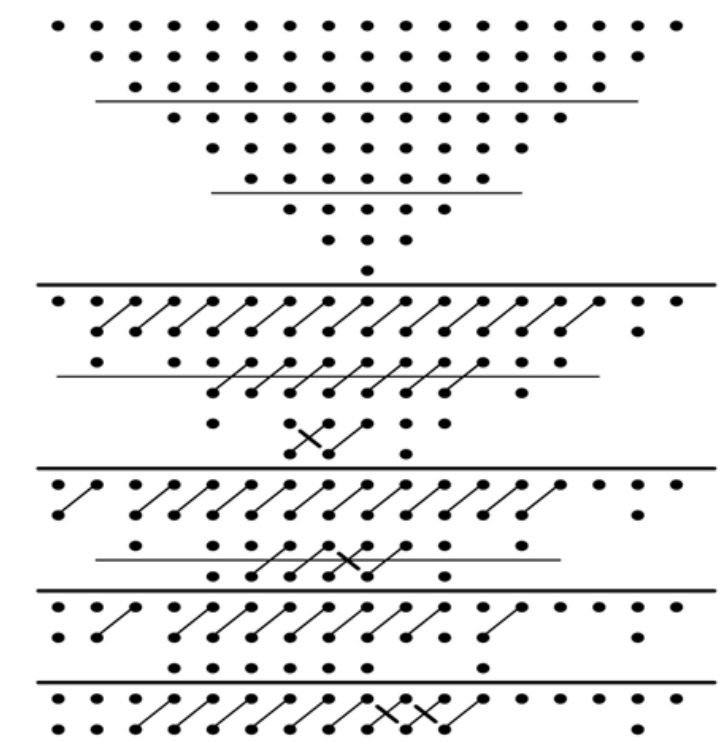

Fig.7. Modified Wallace 9-bit by 9-bit reduction.

The modified Wallace reduction method divides the matrix into three row groups and uses full adders for each group of three bits in a column like the conventional Wallace reduction[6]. A group of two bits in a column is not processed, that is, it is passed on to the next stage (in contrast to the conventional Wallace reduction). Single bits are passed on to the next stage as in the conventional Wallace reduction.

The only time half adders are used is to ensure that the number of stages of the modified Wallace multiplier does not exceed that of a conventional Wallace multiplier. For some cases, half adders are only used in the final stage of reduction. In the 9-bit by 9-bit example, a half adder is used in the first and the second stages to handle partial product terms that, if not addressed, would increase the number of reduction stages and increase the multiplier delay. Also two half adders are used in the final stage. The reduction is performed in four stages (the same as the Wallace reduction) with a total of 52 full adders and four half adders. The third phase will require a 16-bit wide adder. The modified Wallace reduction uses two more full adders and 17 fewer half adders than the conventional Wallace reduction.

6. CMOS SCEMATIC OF WALLACE TREE MULTIPLIER USING LOW POWER AND AREA EFFICIENT FULLADDER

This paper discussion on modified design that greatly reduces the number of half adders in Wallace multipliers.

Initially, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

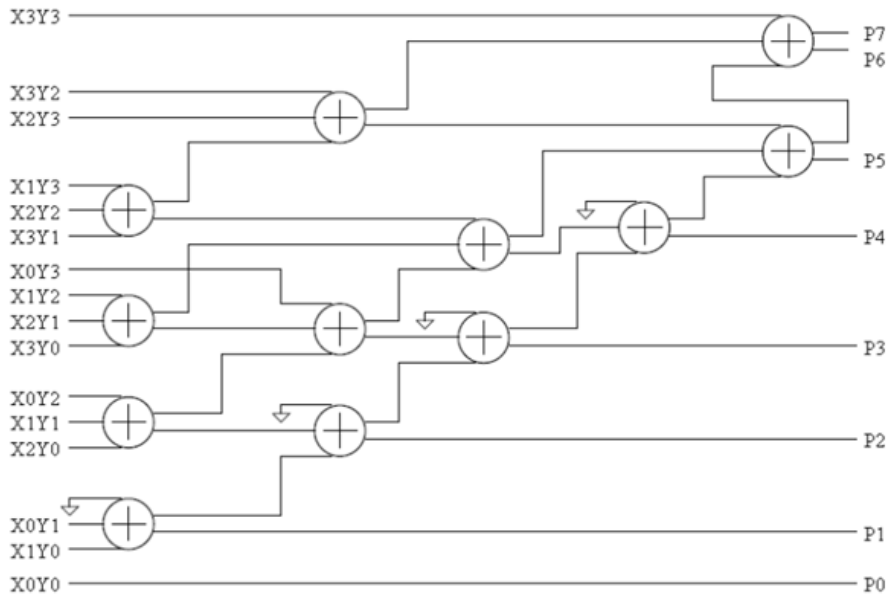

Fig 8 Designed Wallace tree multiplier

Above architecture show proposed Wallace tree multiplier showing 12 full adder. Full adder will be designed using CMOS low power. Design has provide partial product and 8 bit output will be generated.

6.1 Schematic implementation of reduce complexity wallace multiplier

Figure 9. shows the schematic design of modified reduced complexity wallace multiplier. The schematic is design on s-edit by adjoining encoders, modified adder, partial product generator and basicaly some gates like OR,XOR and AND. In this wallace multiplier, the N rows of partial product bits are reduced to two rows. the Wallace approach uses several stages of full and half adders as carry save adders that are arranged to maximize the reduction at each stage. So that complexity get reduced.

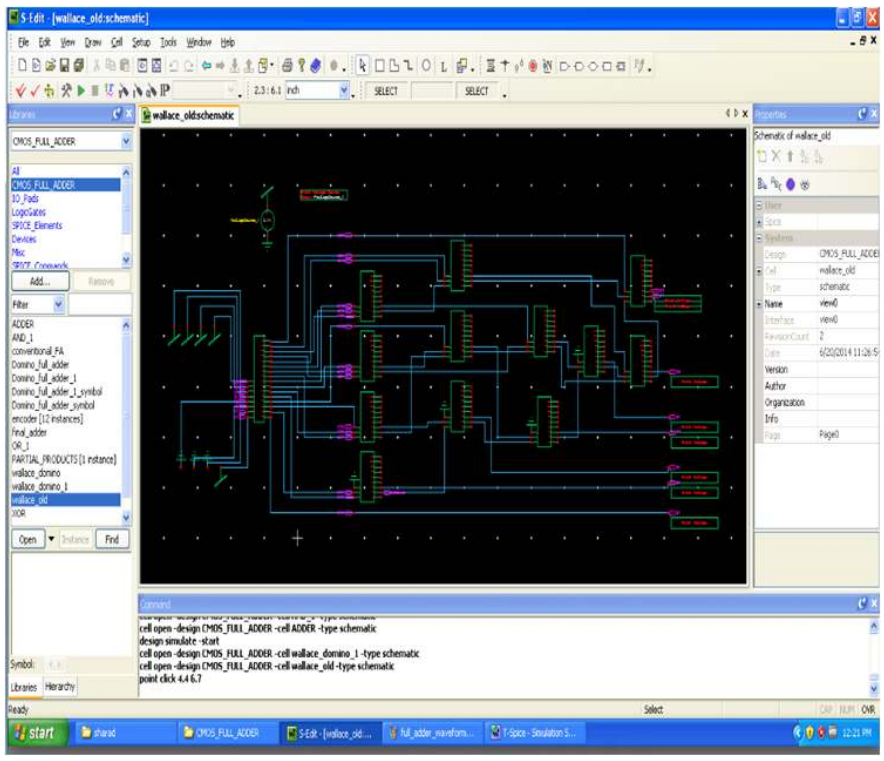

Fig. 9. Modified Wallace multiplier

7. RESULT ANALYSIS OF REDUCED COMPLEXITY WALLACE MULTIPLIER:

Figure.10.shows status of inputs, output and intermediate signals of reduced complexity wallace multiplier using modified full adder in the form of waveform. clock signal has been shown in the form of pulse.

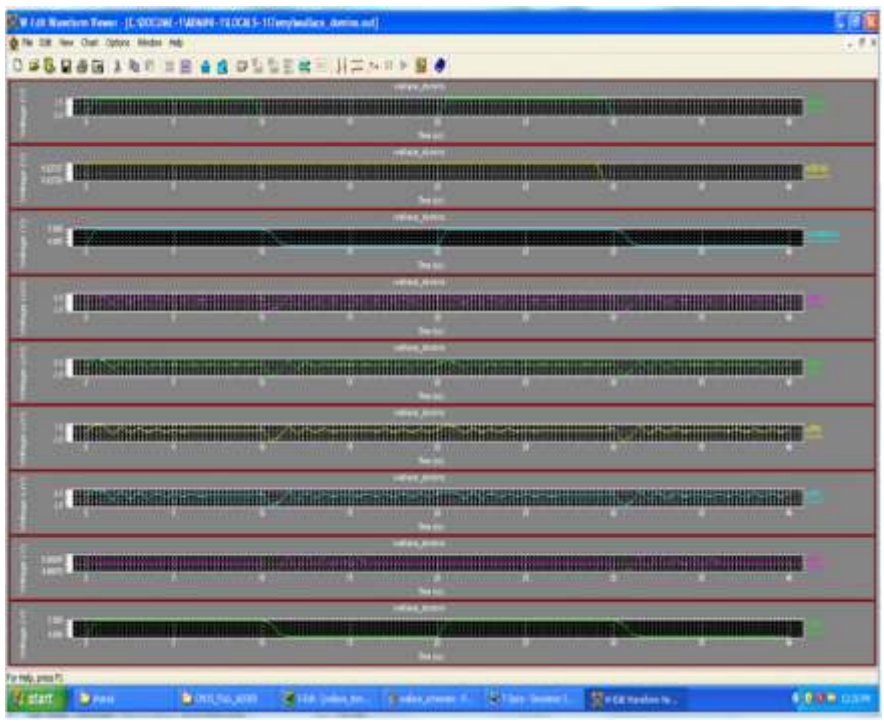

Figure 10. waveform representation of wallace multiplier

Output waveform drawn from w-edit tool of tanner ED. after t-spice simulation, simulation result obtain in the form of waveform.which shows improved speed and less power consumption of the reduce complexity modified Wallace tree multiplier.

From the figure 10, it is clear that no. of half adder required to make modified Wallace multiplier is lesser than conventional Wallace multiplier, but this reduce complexity occurs at the cost slight increase in full adder, so our output 8 bit wallace multiplier required 12 full adder. After comparison of modified Wallace multiplier with dada and previous multipliers over matlab, it is found that modified Wallace multiplier has less complexity[8]. Our modified Wallace approach uses several stages of full and half adders as carry save adders that are arranged to maximize the reduction at each stage.

8.CONCLUSION

- Different logic styles which are used in today's digital circuits were addressed and among them, transmission gate logic and compound domino logic (CDL) were selected to be used in the designed adder in order to achieve high speed and to dissipate as little power as we can.
- An alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, two full-adders were built in combination with pass-transistor powerless/groundless logic styles.
- Propagation delay and power consumption are comparable for small circuits (i.e. circuits with less no. of inputs) in CMOS, pseudo NMOS, Domino and FTL because the device count is low and structure is not cascaded.
- This thesis presents a modification to the second phase reduction (that reduces N rows of bit products to two rows) used in Wallace multipliers. The modified Wallace reduction reduces the number of half adders required by at least 80 percent compared to the conventional Wallace reduction with only a very slight increase in the number of full adders.
- Both the conventional Wallace and modified Wallace reductions have the same number of stages and consequently the delay is expected to be the same. It is significant that both the conventional and modified Wallace second phase reductions use more gates than the Dadda reduction, although the penalty is less for the modified Wallace reduction.
- Simulations showed power savings up to 80%, and speed improvements up to 25%, for a joint optimization of 85% for the PDP. The area utilization for the proposed full-adders is only 40% of the largest full-adder compared, and the power-supply voltage for the proposed full-adders can be lowered down to 0.6 V, maintaining proper functionality.
- Wallace tree multiplier result in fast multiplication and low power design.

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