Research Paper

IONIZING RADIATION INFLUENCE ON 28-NM MOS TRANSISTOR'S LOW-FREQUENCY NOISE CHARACTERISTICS

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ABSTRACT:

In this study, we investigate changes in low-frequency noise characteristics of high-k metal-gate bulk CMOS transistors due to Total Ionizing Dose (TID) exposure. Understanding these changes is complicated by the strong bias dependence of noise characteristics, which makes it difficult to distinguish between shifts caused by effective biasing changes and those due to newly generated traps. To comprehend the effects of irradiation better, transistor noise was analyzed at multiple biasing points in both linear and saturation regions before and after exposure to 1 Grad (SiO_2) of TID. This paper presents correlations between shifts observed in the time and frequency domains, accompanied by possible explanations for each observed variation. We provide examples of Random Telegraph Noise (RTN) defects induced by irradiation and demonstrate the impact of TID on noise Power Spectral Density (PSD) curves containing pre-existing RTN sources.

KEYWORDS: Radiation damage to electronic components; Radiation-hard electronics; Analogue electronic circuits.

INTRODUCTION

The source of Low-Frequency Noise (LFN) in planar MOSFET transistors has been a topic of discussion for more than five decades and remains unresolved today [1–3]. In older technology nodes, this noise exhibits a Power Spectral Density (PSD) curve that decreases proportionally with frequency, leading to its designation as 1/f noise, or more commonly known as flicker noise. As transistor dimensions have shrunk rapidly, Random Telegraph Noise (RTN) with a Lorentzian-shaped PSD has become more prevalent. Both flicker and random telegraph noise are attributed to the trapping and detrapping of charge carriers between the gate oxide and the semiconductor channel. The 1/f noise is often modeled as a sum of numerous individual Lorentzians distributed across all trap locations and energies [4, 5]. In deep sub-micron technologies, the PSD curve typically deviates from a pure 1/f shape, reflecting the presence of contributing traps. In electronic devices subjected to constant stress conditions, such defects are susceptible to alteration over time.

High-energy physics experiments necessitate electronics capable of withstanding ultra-high doses of ionizing radiation reliably. Understanding the impact of irradiation on transistor noise characteristics is crucial for designing radiation-resistant ASICs. The Total Ionizing Dose (TID) expected from the High-Luminosity Large Hadron Collider (HL-LHC) project at CERN could reach up to 1 Grad (SiO_2), serving as a benchmark in our experiments. Previous studies on radiation effects in bulk MOSFETs highlight that transistor performance degradation primarily stems from charge accumulation in gate, STI, and spacer oxides above Lightly Doped Drain (LDD) regions, as well as at the gate channel/oxide interface [6–8].

Initial experiments indicate enhanced radiation tolerance with reduced oxide dimensions. However, as transistor dimensions decrease further, Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects have been observed, revealing decreased TID tolerance [9]. Notably, sub-100 nm transistors exhibit a reversal of the RISCE effect, attributed to increased halo implantation overlap boosting overall doping in the channel region and reducing the impact of trapped oxide charges in the spacer region [10]. These advancements, alongside speed and power consumption improvements, highlight 28-nm CMOS technology as strategically significant for future high-energy physics instrumentation applications [11].

This paper explores how TID influences Low-Frequency Noise (LFN) characteristics in minimum-sized 28 nm technology MOSFETs. Unlike previous studies that primarily address potential shifts in noise Power Spectral Density (PSD) [12, 13], our research covers various scenarios: creation and cessation of dominant Random Telegraph Noise (RTN) defects, alterations in PSD shape, and overall changes in noise levels.

METHODS

The irradiation was conducted using the Seifert XRD Cabinet at room temperature, employing a tungsten tube biased at 40 kV and 70 mA. The distance between the tube shutter and the chip surface was approximately 30 cm, resulting in a dose rate of 6.2 Mrad/h. NMOS and PMOS transistors were biased in a diode configuration with gate and drain terminals set at 0.9/−0.9 V, known to induce worst-case performance degradation under Total Ionizing Dose (TID) influence [9, 14]. The irradiation exposure lasted approximately 7 days to achieve 1 Grad of TID.

Low-frequency noise measurements were taken before and after the irradiation using a custom-built noise measurement setup (see Figure 1), capable of acquiring time- and frequency-domain noise data. To prevent annealing effects, no intermediate measurements were taken during irradiation. The noise power spectral density of drain current was calculated by averaging Fast Fourier Transform (FFT) data from 80 one-second time windows sampled at 2 GSa/s. Frequency domain signals were observed between 10 Hz and 100 kHz, limited by internal low-pass and high-pass filters of the measurement system. DC measurements were also conducted to determine threshold voltage and sub-threshold slope shifts.

The devices used in these experiments were high-k, Si bulk, commercial 28-nm transistors with minimum-sized dimensions (W/L = 100 nm/30 nm and 100 nm/40 nm). To minimize the influence of ESD protection leakage current on measurements, a reduced ESD concept was implemented, resulting in damage to several devices during the study, with PMOS transistors exhibiting a higher survival rate. The examples presented in this study were derived from 30 irradiated and measured devices.

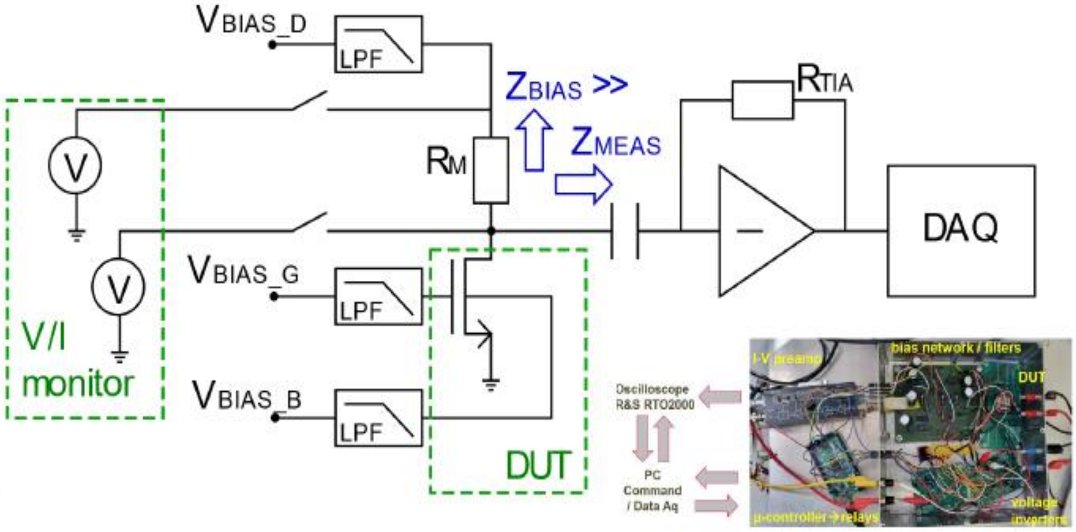

Figure 1. Noise measurement system; electrical diagram and test bench photo.

RESULTS AND DISCUSSION

Given the substantial variability in noise characteristics among transistors of identical geometries and biasing conditions (illustrated in Figures 2a and 2b), achieving a comprehensive statistical understanding of the impact of irradiation necessitates a large number of experiments. This paper, however, primarily aims to offer a qualitative exploration of the potential effects of Total Ionizing Dose (TID) on individual cases.

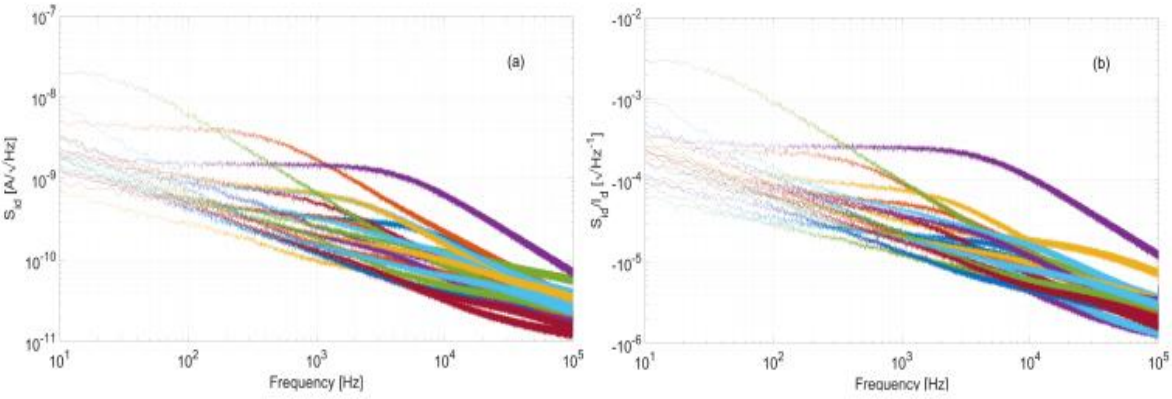

Figure 2. Absolute (a) and scaled (b) current spectral density of non-irradiated PMOS transistors with W/L = 100/30 nm, biased at Vgs = −0.7 V, Vds = −0.05 V.

Normalizing the current noise spectral density by the drain DC current is a widely adopted method for pre- and post-stressing analysis. This approach is particularly effective for Power Spectral Density (PSD) spectra exhibiting 1/f-like curve shapes, where established noise models [15, 16] suggest that factoring in the DC current mitigates differences in noise PSD caused by degradation in DC parameters due to Total Ionizing Dose (TID). Our investigations corroborate the findings of previous studies [17], highlighting distinct bias dependence between individual Random Telegraph Noise (RTN) defects and the cumulative noise contribution of multiple defects, which often manifests as a 1/f-like characteristic.

Therefore, we employ normalized current PSD to illustrate TID-induced shifts in noise levels, while absolute current PSD is used to demonstrate changes in RTN behavior. In most cases, the primary effect of TID on noise PSD (as shown in Figure 3a) is an increase in normalized PSD. However, in a minority of cases, the PSD may remain unaffected or even decrease (as shown in Figure 3b), which can be attributed to the shutdown of defects induced by irradiation. This phenomenon will be further discussed in the subsequent section.

In most observed cases, besides causing level shifts, irradiation alters the shape of noise PSD curves. These changes result from fluctuations in the behavior of single traps.

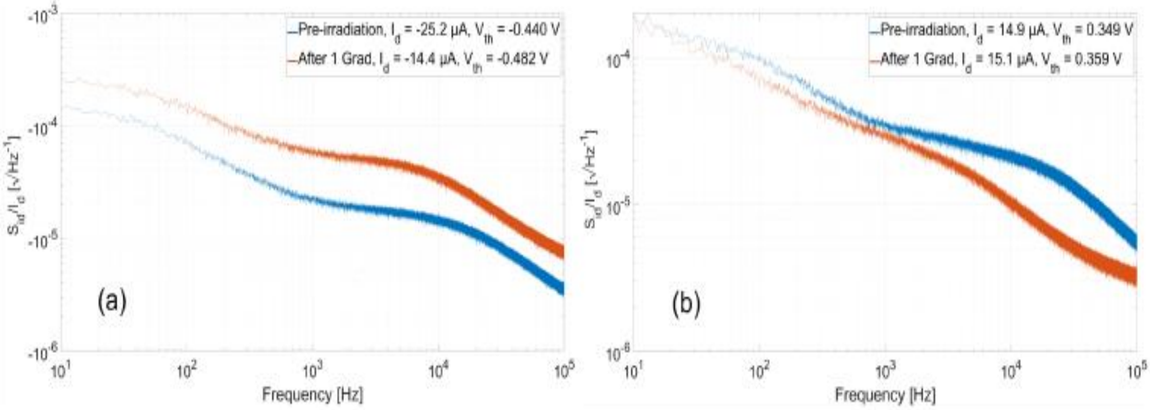

Figure 3. Examples of scaled current spectral density increase (a) and decrease (b) after exposure to 1 Grad (SiO_2) TID. (a) PMOS transistors with W/L = 100/40 nm, biased at Vgs = −0.7 V, Vds = −0.4 V. (b) NMOS transistors with W/L = 100/30 nm, biased at Vgs = 0.5 V, Vds = 0.4 V.

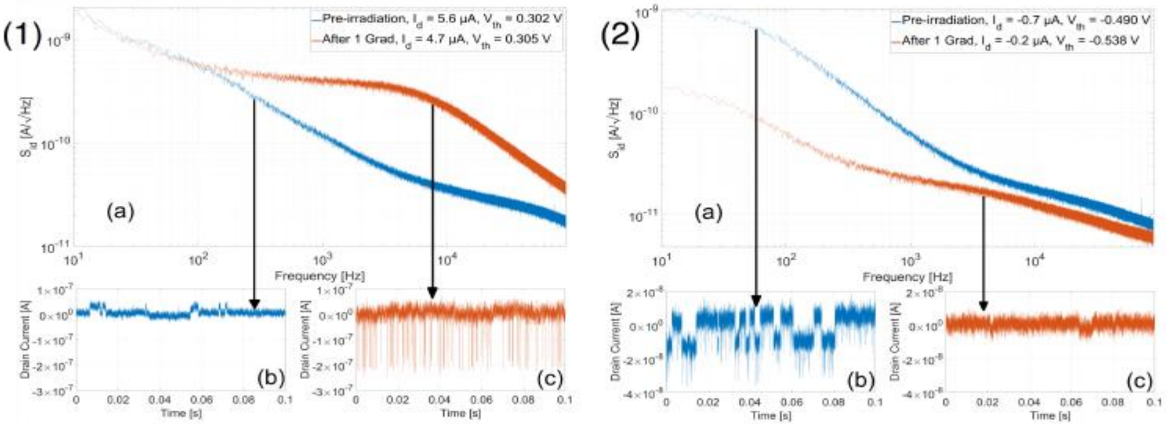

Figure 4. Example of an irradiation-induced dominant RTN center in frequency (a) and time domain (b and c). NMOS transistors with W/L = 100/30 nm, biased at Vgs = 0.5 V, Vds = 0.05 V.

A typical example is the emergence of a prominent RTN defect activation (see Figure 4(1)). Random telegraph noise is recognizable for its characteristic behavior of exhibiting discrete, two- or multi-step jumps in drain current in the time domain. In the frequency domain, RTN manifests as a Lorentzian-shaped curve, initially flat, then transitioning through a corner frequency, followed by a drop resembling $1/f^2$. The corner frequency of an RTN Lorentzian curve is determined using equation (3.1), where $\overline{T}_c$ represents the average time for the trap to capture electric charge and $\overline{T}_e$ denotes the time for it to emit it back to the channel [18].

$$f_c = \frac{1}{2\pi}\left(\frac{1}{\overline{T}_e}+\frac{1}{\overline{T}_c}\right) \tag{3.1}$$

Another observed phenomenon, depicted in figure 4(2), shows the reverse effect compared to that in figure 4(1): the RTN center ceases to capture charge at the same biasing point after irradiation. Possible causes could involve one or a combination of known oxide degradation mechanisms considered in bias temperature instability models [19]. These mechanisms include transformations of preexisting oxide defects (either in energy or physical location) due to hydrogen relocation, generation and annealing of oxide defects, as well as passivation and activation of dangling bonds.

Since transistors undergo Total Ionizing Dose (TID) stress under bias, which also induces self-heating, the bias temperature effect interacts with high TID radiation stress. These combined effects have not been fully separated in studies, indicating a need for further investigation into their interactions.

To compensate for the overall biasing shift, prior studies employed DC drain current scaling. However, our findings indicate that individual RTN defects may exhibit different bias dependencies compared to 1/f-like noise. Therefore, using this scaling method could distort results. Instead, for a clearer understanding of radiation's impact on single RTN defects, more accurate outcomes can be achieved by biasing the transistor with a voltage that compensates for the threshold voltage shift.

In figure 5b, biasing compensation following TID exposure involved adjusting the gate voltage to offset the Vth shift and tuning the drain voltage to maintain the same Id as pre-stressing levels. The latter adjustment is often impractical due to TID-induced decreases in ION. The results from figure 5b indicate that in this case, the trap did not disappear as suggested by measurements at the same biasing point post-irradiation. Instead, it ceased to capture and emit charge due to the transistor's net biasing change.

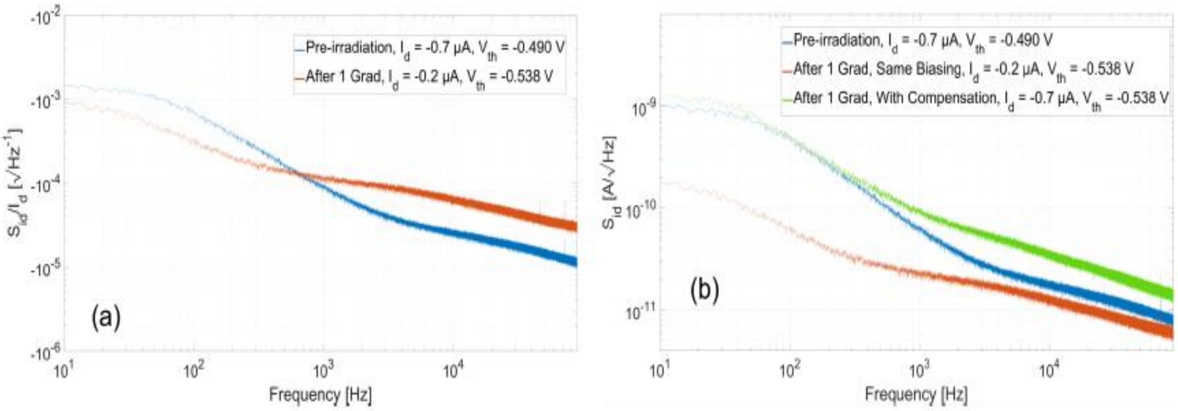

Figure 5. Comparison between the Id-scaled current spectral density (a) and unscaled where compensation for the V_{th} shift is added (b). PMOS transistors with W/L = 100/40 nm, biased at Vgs = −0.5 V, Vds = −0.05 V before and at Vgs = −0.548 V, Vds = −0.09 V after compensation.

Furthermore, analysis of the remaining noise spectrum showed an increase after bias compensation, similar in scale to what is observed in figure 5a, suggesting an increase in defect numbers due to TID exposure.

This method is valuable for studying changes in RTN behavior resulting from TID-induced biasing shifts but has limitations in identifying the underlying reasons for RTN shutdown. Additionally, to accurately analyze the effects of irradiation on individual RTN traps, it is crucial to distinguish between changes in noise PSD caused by net biasing alterations and those arising from the creation of new defects.

CONCLUSION

The noise current spectral density characteristics of 28-nm CMOS transistors exhibit significant variability prior to Total Ionizing Dose (TID) stress. We illustrate how these characteristics evolve after exposure to ultrahigh doses of ionizing radiation. Our measurements on multiple PMOS and NMOS transistors reveal instances of both increased and decreased noise PSD under identical bias conditions before and after TID stress. This variability is attributed to the likelihood of dominant Random Telegraph Noise (RTN) occurrences, their bias dependence, and the intricate oxide degradation phenomena induced by TID stress.

The disparity in bias dependence between 1/f noise PSD and RTN amplitude suggests that both absolute noise PSD and normalized noise PSD with respect to DC current variation need to be considered when analyzing low-frequency noise characteristics. Additionally, our findings indicate that analyzing at a fixed biasing point can be misleading due to the TID-induced shift in threshold voltage coupled with the strong bias dependence of RTN.

Further investigations should focus on gaining a deeper understanding of 1/f noise mechanisms in very small devices, developing a comprehensive physical model of RTN traps, and exploring the interrelationships between these factors.

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